Features

- Ultra High Performance
  - System Speeds to 100MHz
  - Array Multipliers > 50MHz
  - 10ns Flexible SRAM
  - Internal 3-State Capability in each Cell
- FreeRAM™
  - Flexible, Single/Dual Port, Sync/Async 10ns SRAM
  - 2,048 - 18,432 Bits of Distributed SRAM Independent of Logic Cells
- 84 - 384 PCI Compliant I/Os
  - 3V/5V Capability
  - Programmable Output Drive
  - Fast, Flexible Array Access Facilitates Pin-Locking
  - Pin Compatible with XC4000, XC5200 FPGAs
- 8 Global Clocks
  - Fast, Low Skew Clock Distribution
  - Programmable Rising/Falling Edge Transitions
  - Distributed Clock Shut-Down Capability for Low Power Management
  - Global Reset/Asynchronous Reset Options
  - 4 Additional Dedicated PCI Clocks
- Cache Logic® Dynamic Full/Partial Reconfigurability In-System
  - Unlimited Reprogrammability via Serial or Parallel Modes
  - Enables Adaptive Designs
  - Enables Fast Vector Multiplier Updates
  - QuickChange™ Tools for Fast, Easy Design Changes
- Pin-Compatible Package Options
  - Plastic Leaded Chip Carriers (PLCC)
  - Thin, Plastic Quad Flat Packs (VQFP, TQFP, PQFP)
  - Ball Grid Arrays (BGA)
  - Pin Grid Arrays (PGAs)
- Industry-Standard Design Tools
  - Seamless Integration (Libraries, Interface, Full Back-Annotation) with Concept, Everest, Exemplar, Mentor, OrCAD, Synario, Synopsys, Verilog, Veribest
  - Timing Driven Placement & Routing
  - Automatic/Interactive Multi-Chip Partitioning
  - Fast, Efficient Synthesis
  - Over 50 Automatic Component Generators Create 1000's of reusable, fully deterministic logic functions
- Intellectual Property Cores
  - Fir Filters, UARTs, PCI and other System Level Functions
- Easy Migration to Atmel Gate Arrays for High Volume Production

Device	AT40K05	AT40K10	AT40K20	AT40K30	AT40K40
Usable Gates	5K - 10K	10K - 20K	20K - 30K	30K - 40K	40K - 50K
RowsXColumns	16X16	24X24	32X32	40X40	48X48
Cells	256	576	1,024	1,600	2,304
Registers	256	576	1,024	1,600	2,304
RAM Bits	2,048	4,608	8,192	12,800	18,432
I/O (max)	128	192	256	320	384

AT40K FPGAs

AT40K05
AT40K10
AT40K20
AT40K30
AT40K40

Rev. 0896A-A–12/97

Description

The AT40K is a family of fully PCI-compliant, SRAM-based FPGAs with distributed 10ns programmable synchronous/asynchronous, dual port/single port SRAM, 8 global clocks, Cache Logic ability (partially or fully reconfigurable without loss of data), automatic component generators, and range in size from 5,000 to 50,000 usable gates. I/O counts range from 128 to 384 in industry standard packages ranging from 84-pin PLCC to 475-pin BGA, and support 3V and 5V designs.

The AT40K is designed to quickly implement high performance, large gate count designs through the use of synthesis and schematic-based tools used on a PC, Sun and HP platform. Atmel's design tools provide seamless integration with industry standard tools from Cadence (Concept/Verilog), Everest, Exemplar, Mentor, OrCAD, Synario, Veribest, and Viewlogic.

The AT40K can be used as a Coprocessor for high speed (DSP/Processor-based) designs by implementing a variety of compute-intensive, arithmetic functions. These include adaptive finite impulse response (FIR) filters, fast Fourier transforms (FFT), convolvers, interpolators and discrete-cosine transforms (DCT) that are required for video compression and decompression, encryption, convolution and other multimedia applications.

Fast, Flexible and Efficient SRAM

The AT40K FPGA offers a patented distributed 10ns SRAM capability where the RAM can be used without losing logic resources. Multiple independent, synchronous or asynchronous, dual port or single port RAM functions (FIFO, scratch pad, etc.) can be created using Atmel's macro generator tool.

Fast, Effecient Array & Vector Multipliers

The AT40K's patented 8-sided core cell with direct horizontal, vertical and diagonal cell-to-cell connections implements ultra fast array multipliers without using any busing resources. The AT40K's Cache Logic capability enables a large number of design coefficients and variables to be implemented in a very small amount of silicon, enabling vast improvement in system speed at much lower cost than conventional FPGAs.

Cache Logic Design

The AT40K is only FPGA family capable of implementing Cache Logic (Dynamic full/partial logic reconfiguration, without loss of data, on-the-fly) for building adaptive logic and systems. As new logic functions are required, they can be loaded into the logic cache without losing the data already there or disrupting the operation of the rest of the chip; replacing or complementing the active logic. The AT40K can act as a reconfigurable coprocessor.

Automatic Component Generators

The AT40K is the only FPGA family capable of implementing user-defined, automatically generated, macros in multiple designs; speed and functionality are unaffected by the macro orientation or density of the target device. This enables the fastest, most predictable and efficient FPGA design approach and minimizes design risk by reusing already proven functions. The Automatic Component Generators work seamlessly with industry standard schematic and synthesis tools to create the fastest, most efficient designs available.

The patent-pending AT40K Series architecture employs a symmetrical grid of small yet powerful cells connected to a flexible busing network. Independently controlled clocks and resets govern every column of cells. The array is surrounded by programmable I/O.

Devices range in size from 5,000 to 50,000 usable gates in the initial family, and 256 to 2,304 registers. Pin locations are consistent throughout the AT40K Series for easy design migration in the same package footprint. AT40K Series FPGAs utilize a reliable 0.6 mm single-poly, triple-metal CMOS process and are 100% factory-tested. Atmel's PC- and workstation-based Integrated Development System is used to create AT40K Series designs. Multiple design entry methods are supported.

The Atmel architecture was developed to provide the highest levels of performance, functional density and design flexibility in an FPGA. The cells in the Atmel array are small, efficient and can implement any pair of Boolean functions of (the same) three inputs or any single Boolean function of four inputs. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances

The Symmetrical Array

At the heart of the Atmel architecture is a symmetrical array of identical cells (Figure 1). The array is continuous from one edge to the other, except for bus repeaters spaced every four cells (Figure 2). At the intersection of each repeater row and column is a 32X4 RAM block accessible by adjacent buses. The Ram can be configured as either a single-ported or dual-ported RAM, with either synchronous or asynchronous operation.

Figure 1. Symmetrical Array Surrounded by I/O (AT40K20)

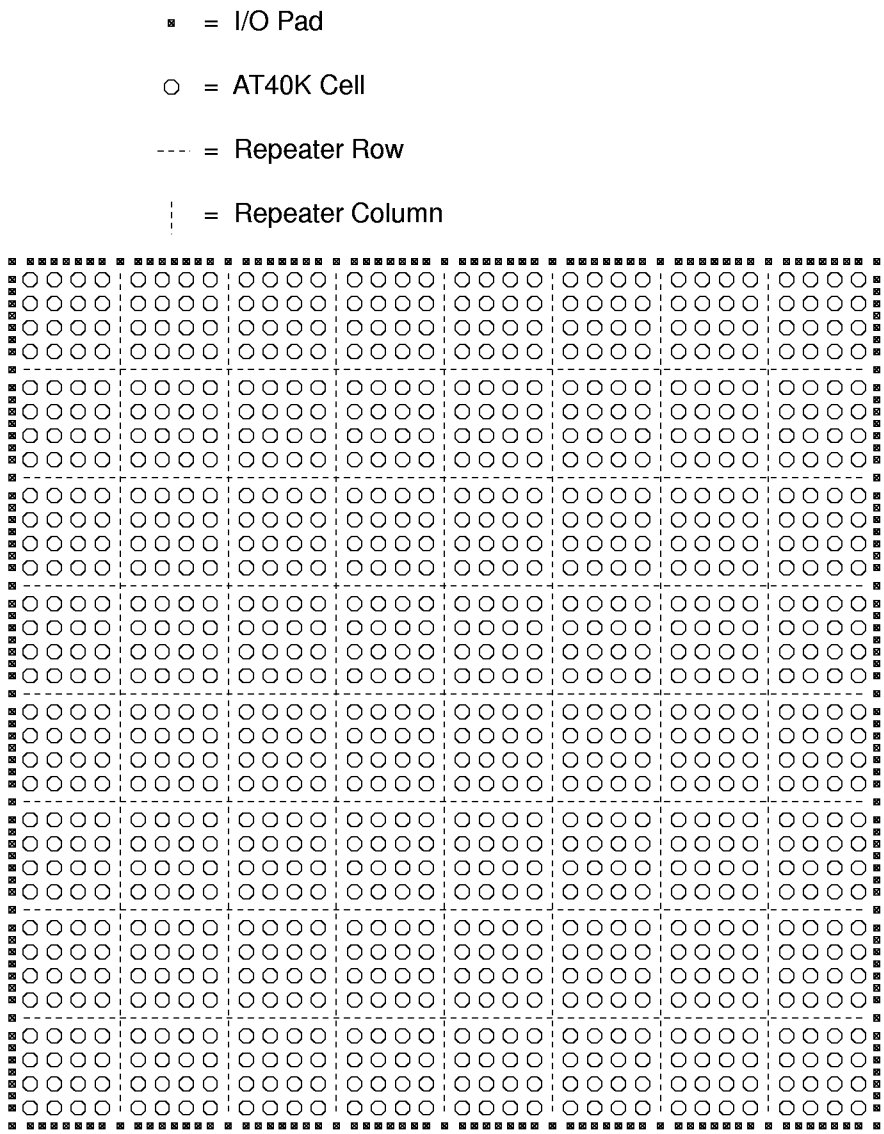
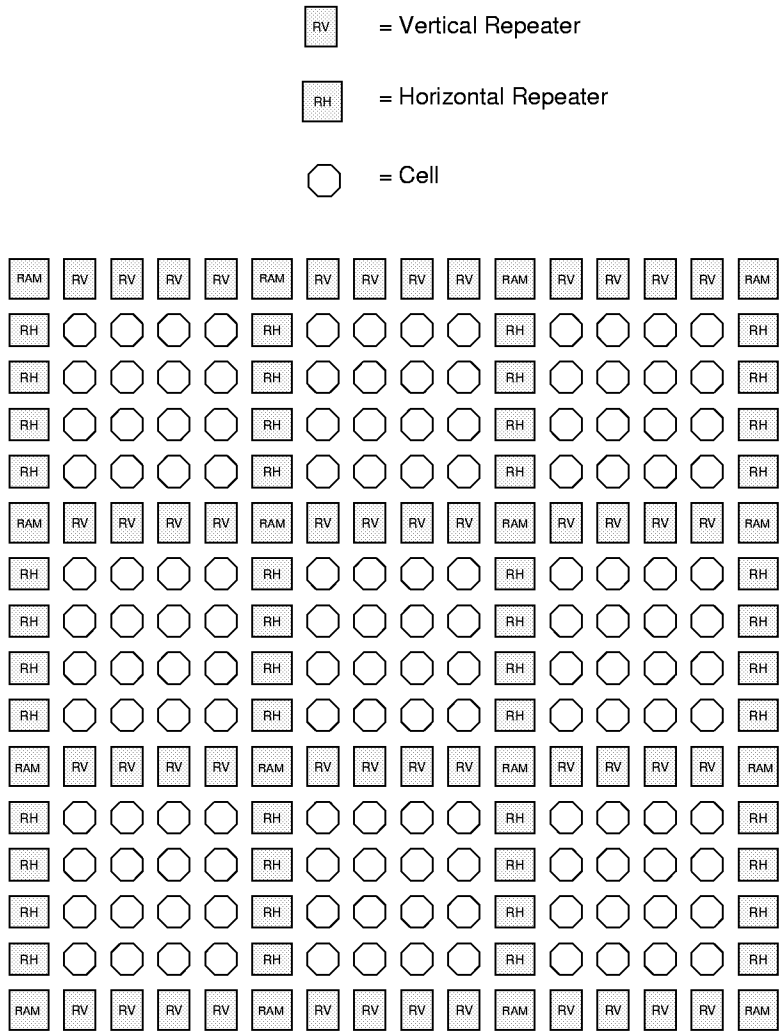


Figure 2. Floorplan (Representative portion)

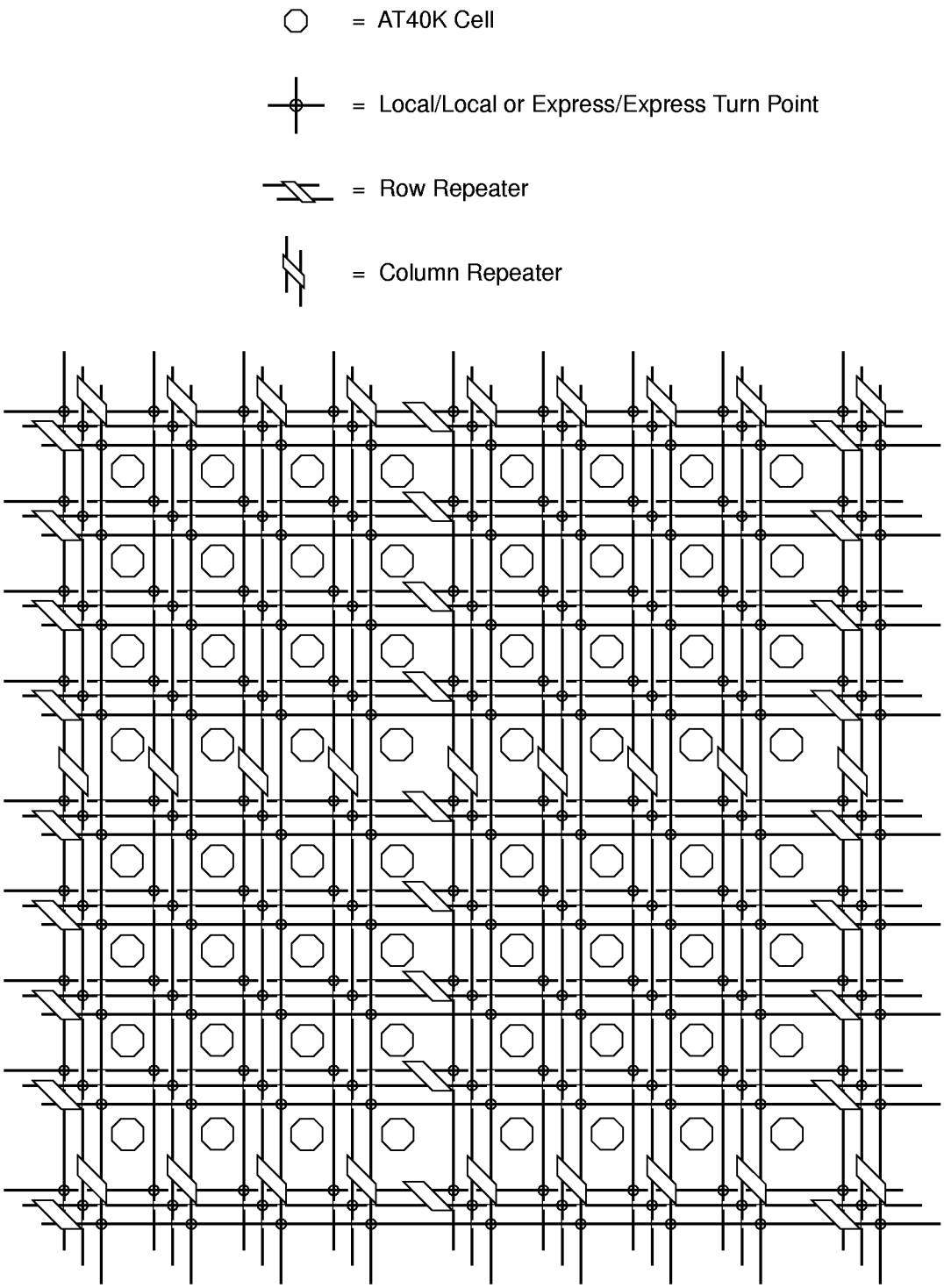


The Busing Network

Figure 3 depicts one of five identical busing planes. Each plane has 3 bus resources: a local-bus resource (the middle bus) and 2 express-bus resources. Bus resources are connected via repeaters. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. Each local-bus segment spans four cells and connects to consecutive repeaters. Each express-bus segment spans eight cells and “leapfrogs” or bypasses a repeater.

Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Although not shown, a local bus can bypass a repeater via a programmable pass gate allowing long on-chip three state buses to be created. Local/Local turns are implemented thru pass gates in the cell-bus interface (see below). Express/Express turns are implemented thru separate pass gates distributed throughout the array.

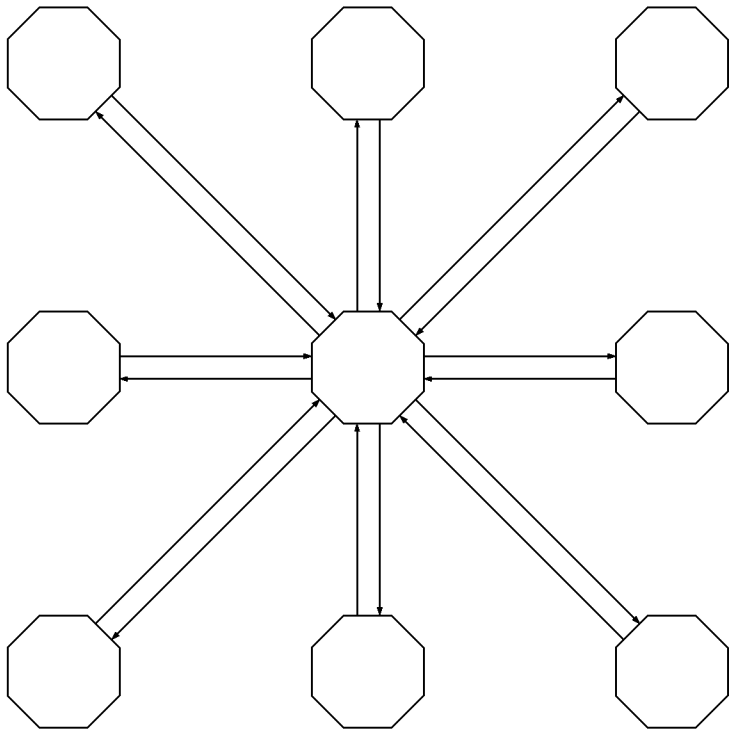
Figure 3. Busing Plane (One of five)



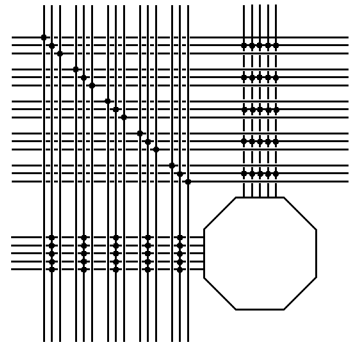
Cell Connections

Figure 4(a) depicts direct connections between a cell and its eight nearest neighbors. Figure 4(b) shows the connections between a cell five horizontal local buses (one per busing plane) and five veritical local buses (one per busing plane).

Figure 4. Cell Connections



(a) Cell to Cell Connections

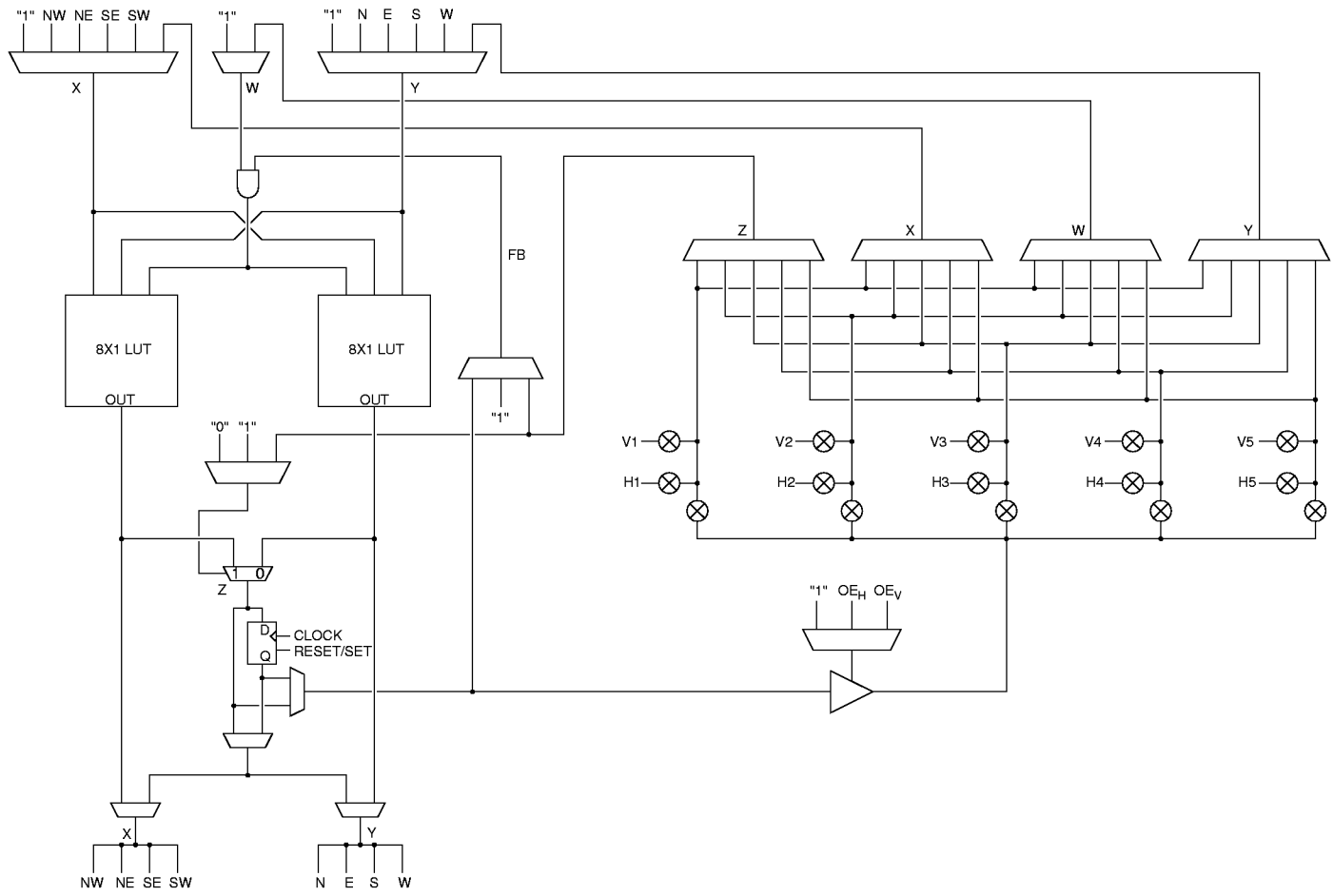


(b) Cell to Bus Connections

The Cell

Figure 5 depicts the AT40K cell. Configuration bits for separate muxes and pass gates are independent. All permutations of programmable muxes & pass gates are legal. Vn is connected to the vertical local bus in plane n. Hn is connected to the horizontal local bus in plane n. A local/local turn in plane n is achieved by turning on the two pass gates connected to Vn and Hn. Up to five simultaneous local/local turns are possible.

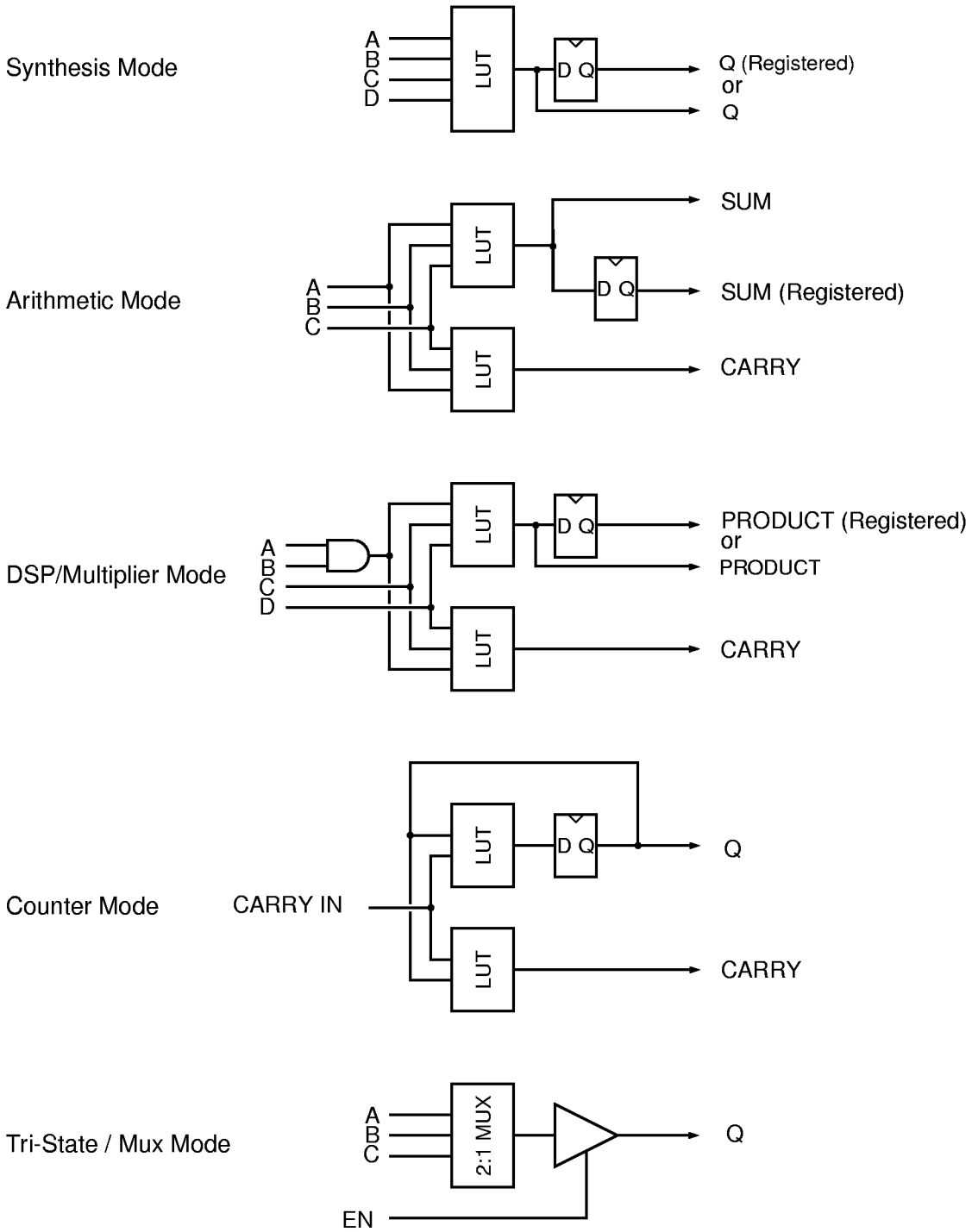
Figure 5. The Cell



X = Diagonal Direct Connect or Bus
Y = Orthogonal Direct Connect or Bus
W = Bus Connection
Z = Bus Connection
FB = Internal Feedback

The core cell can be configured in several “modes”. The core cell flexibility makes the AT40K architecture well suited to most digital design application areas (see Figure 6).

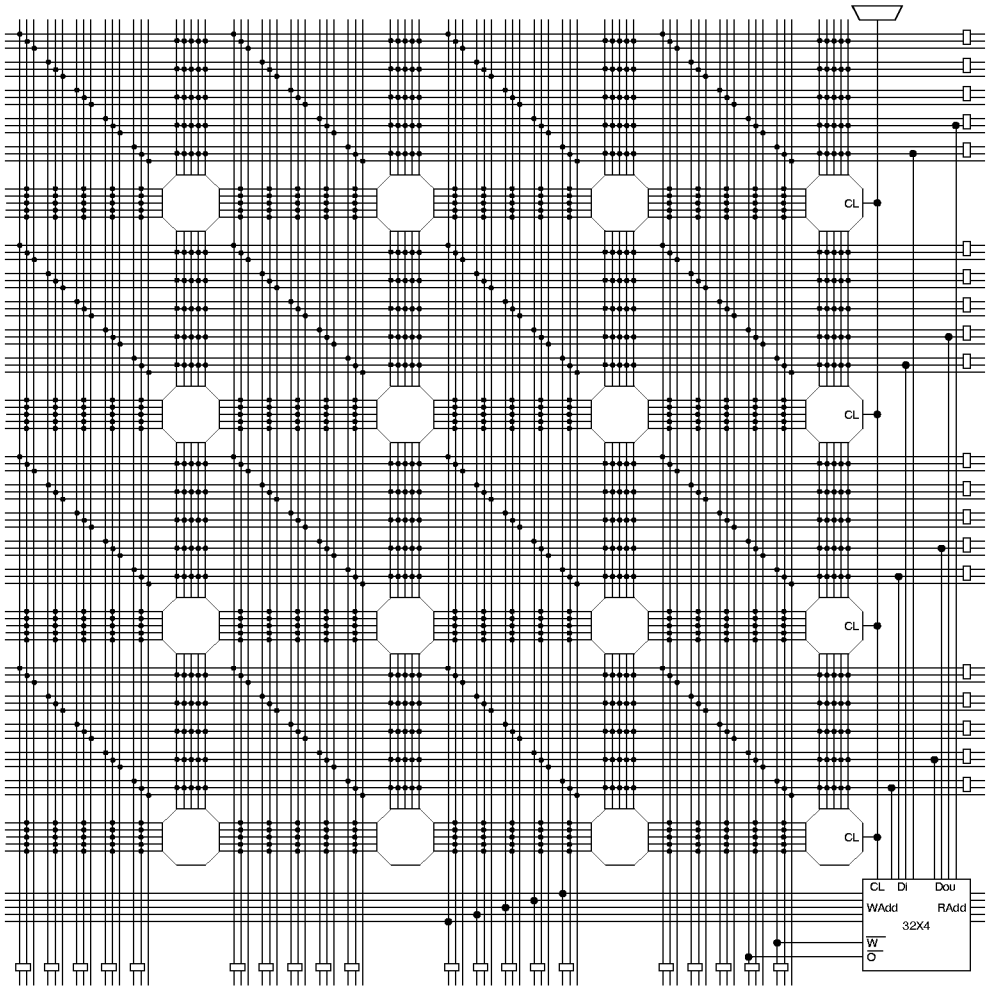
Figure 6. Single Cell Modes



RAM

32X4 Dual-Ported RAM blocks are dispersed throughout the array as shown in Figure 7. A Four-bit Input Data Bus connects to four horizontal local buses distributed over four sector rows. A Four-bit Output Data Bus connects to four horizontal local buses distributed over four sector rows. A Five-bit Input-Address Bus connects to five vertical express buses in same column. A Five-bit Output-Address Bus connects to five vertical express buses in same column. WAddr (Write Address) and RAddr (Read Address) alternate positions in horizontally aligned RAM blocks. For the left-most RAM blocks, RAddr is on the left and WAddr is on the right. For the right-most RAM blocks, WAddr is on the left and RAddr is tied off. For single-ported RAM, WAddr is the READ/WRITE address port and Din is the (bi-directional) data port. Right-most RAM blocks can be used only for single-ported memories. /WE & /OE connect to the vertical express buses in the same column. WAddr, RAddr, /WE and /OE connect to express buses that are full length at array edge.

Figure 7. RAM Connections (One Ram Block)



Reading and writing the 32X4 Dual-Port RAM are independent of each other. Reading the 32X4 Dual-Port RAM is completely asynchronous. Latches are transparent; when Load is logic 1, data flows through; when Load is logic 0, data is latched. Each bit in the 32X4 Dual-Port RAM is a transparent latch. When a Bit = 7 Nibble is (Write) addressed and LOAD is Logic 1 and $\overline{WE}$ is logic 0, DATA flows through the bit. When a nibble is not (Write) addressed or LOAD is logic 0 or $\overline{WE}$ is logic 1, DATA is latched in the nibble. The two CLOCK muxes are controlled together; they both select CLOCK or they both select "1". CLOCK is obtained from the clock for the sector-column immediately to the left and immediately above the RAM block. Writing any value to the RAM Clear Byte during configuration clears the RAM (see Bit Map Spec).

Figure 8. RAM Logic

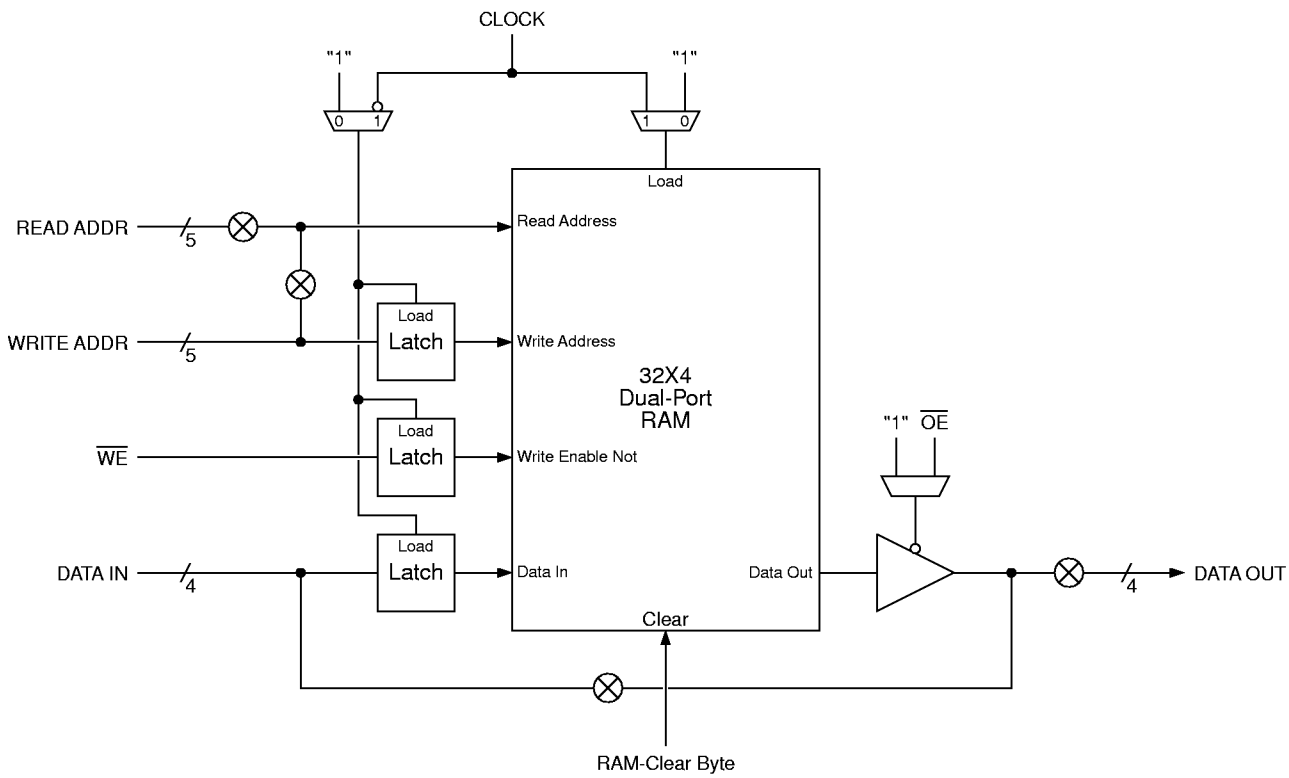
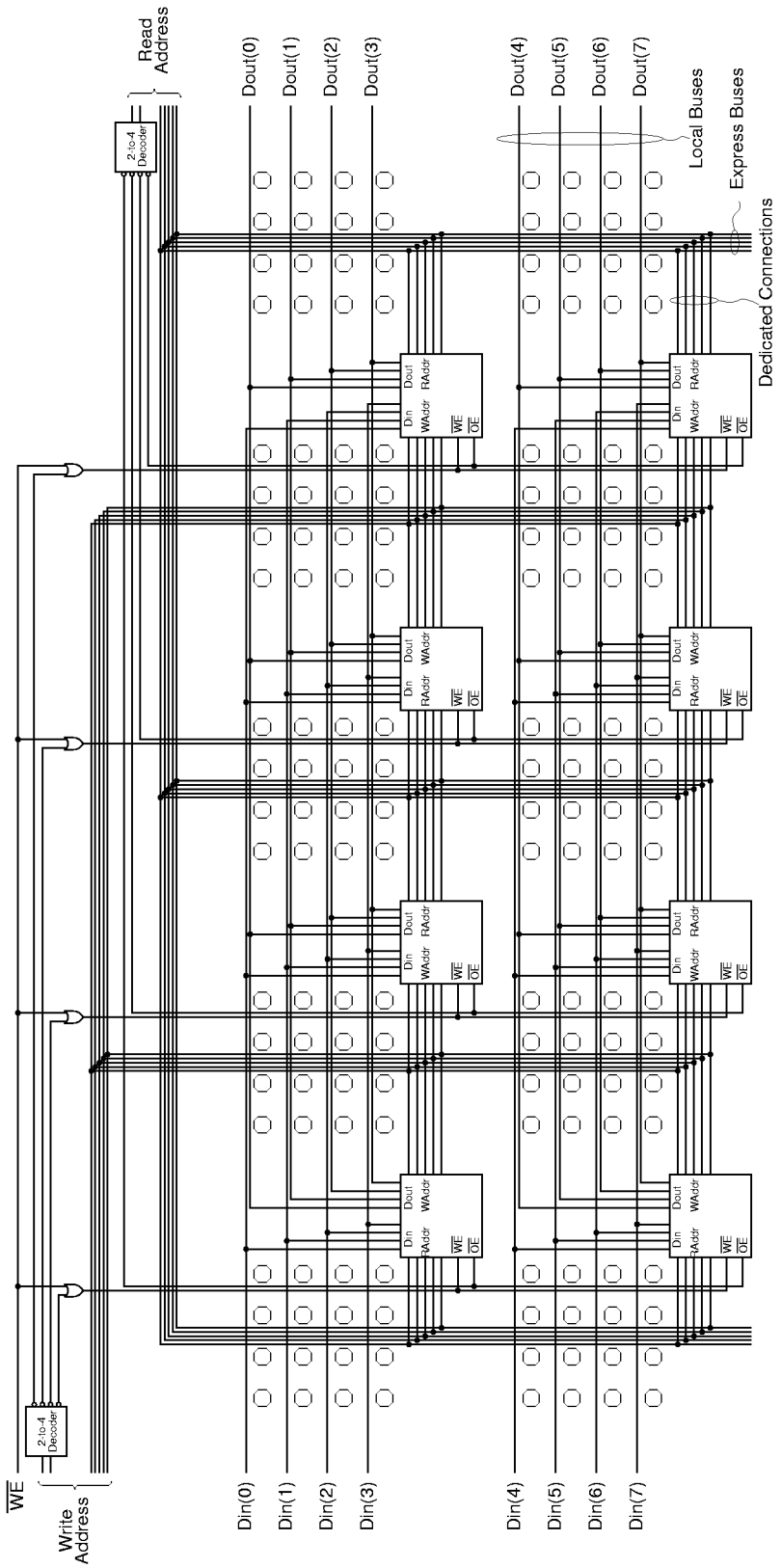


Figure 9. RAM Example: 128X8 Dual-Ported RAM (asynchronous)



Clocking and Set/Reset

Each of 8 dedicated Global Clock buses is connected to a dual-use Global Clock pads (GCK1 = GCK8). An internal signal can be placed on a Global Clock bus by routing that signal to a Global Clock pad. Each column of the array has a Column Clock selected from one of the 8 Global Clock buses. The extreme-left Column Clock mux has two additional inputs from dual-use pins FCK1 & FCK2 to provide fast clocking to left-side I/O. The extreme-right Column Clock mux has two additional inputs from dual-use pins FCK3 & FCK4 to provide fast clocking to right-side I/O. Each sector column of 4 cells can be clocked from a (Plane 4) express bus or from the Column Clock. Clocking to the 4 cells can be disabled. The Plane 4 express bus used for clocking is half length at the array edge. The clock provided to each sector column of 4 cells can be either inverted or not inverted. The register in each cell is triggered on a rising clock edge. On power up, constant “0” is provided to each registers clock pins.

A dedicated Global Set/Reset bus can be driven by any USER I/O pad, except those used for clocking, Global or Fast. An internal signal can be placed on the Global Set/Reset bus by routing that signal to the pad programmed as the Global Set/Reset input. Global Set/Reset is distributed to each column of the array. Each sector column of 4 cells can be Set/Reset by a (Plane 5) express bus or by the Global Set/Reset. The Plane 5 express bus used for Set/Reset is half length at array edge. The Set/Reset provided to each sector column of 4 cells can be either inverted or not inverted. The function of the Set/Reset input of a register (either Set or Reset) is determined by a configuration bit in each cell. The Set/Reset input of a register is Active Low (logic 0). Setting or resetting of a register is asynchronous. On power up, logic 0 (a low) is provided to each register.ie. All registers are Reset at Power up.

Figure 10. Clocking (for one column of cells)

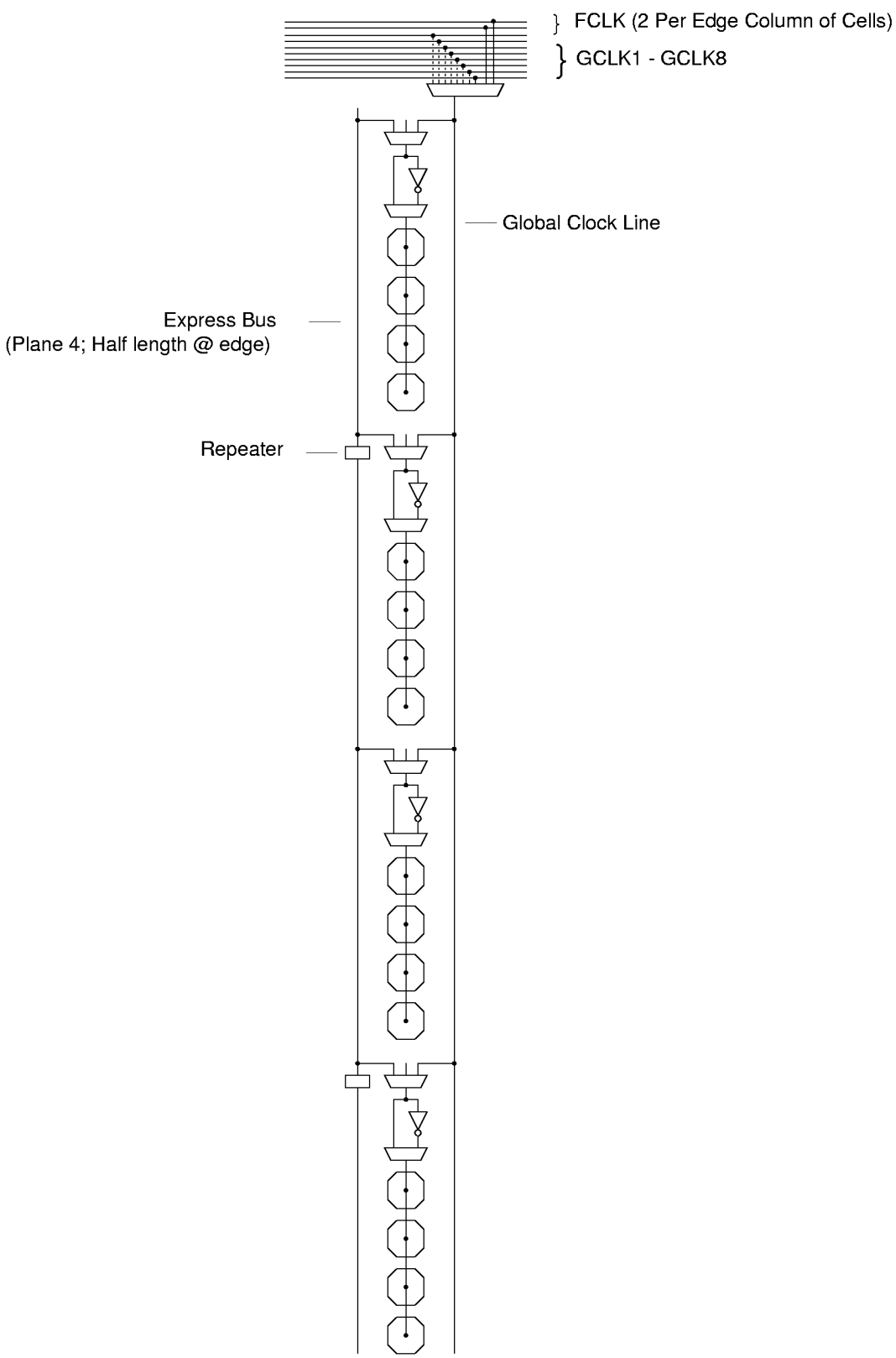


Figure 11. Set/Reset (for one column of cells)

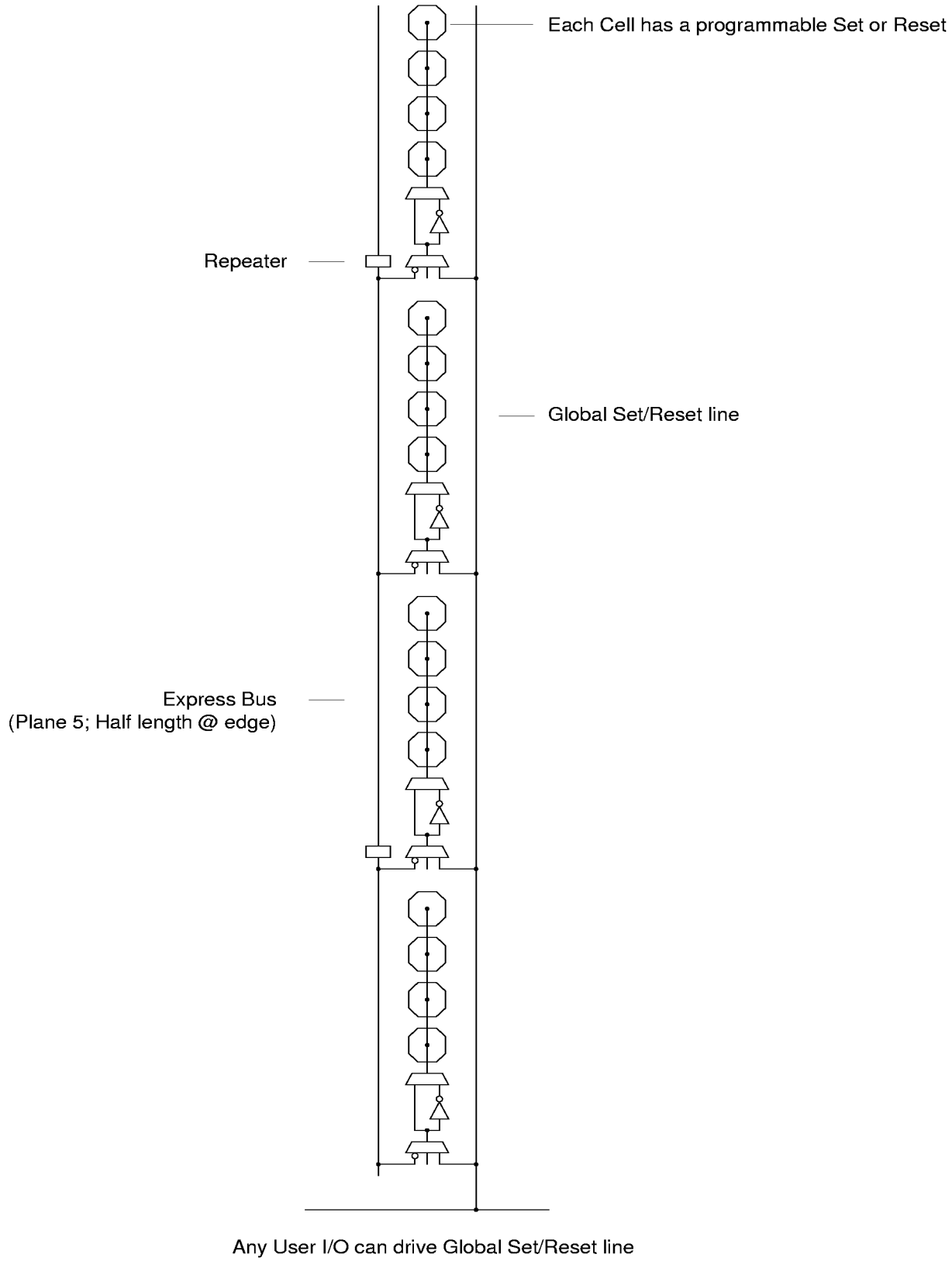
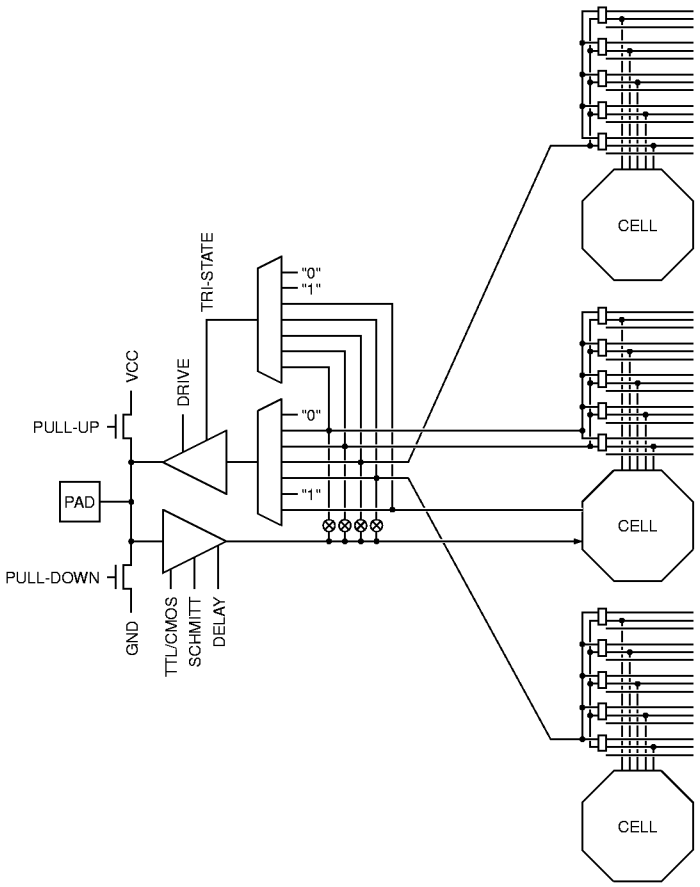
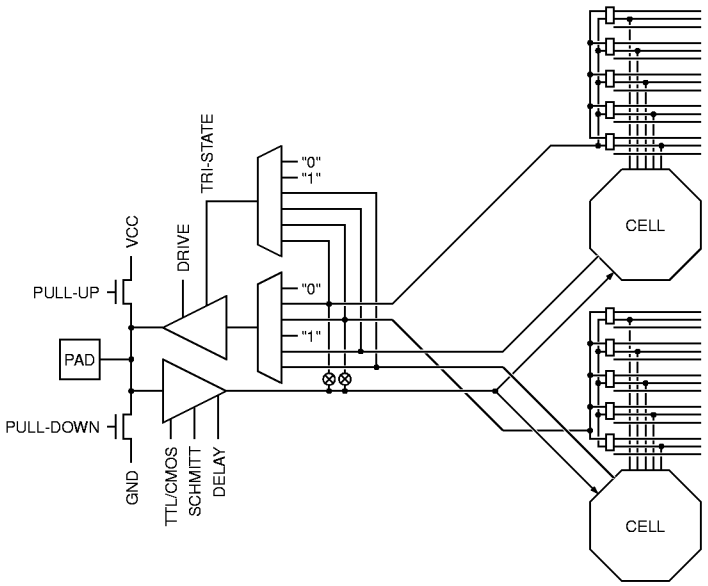


Figure 12. West I/O (Mirrored for EastI/O)

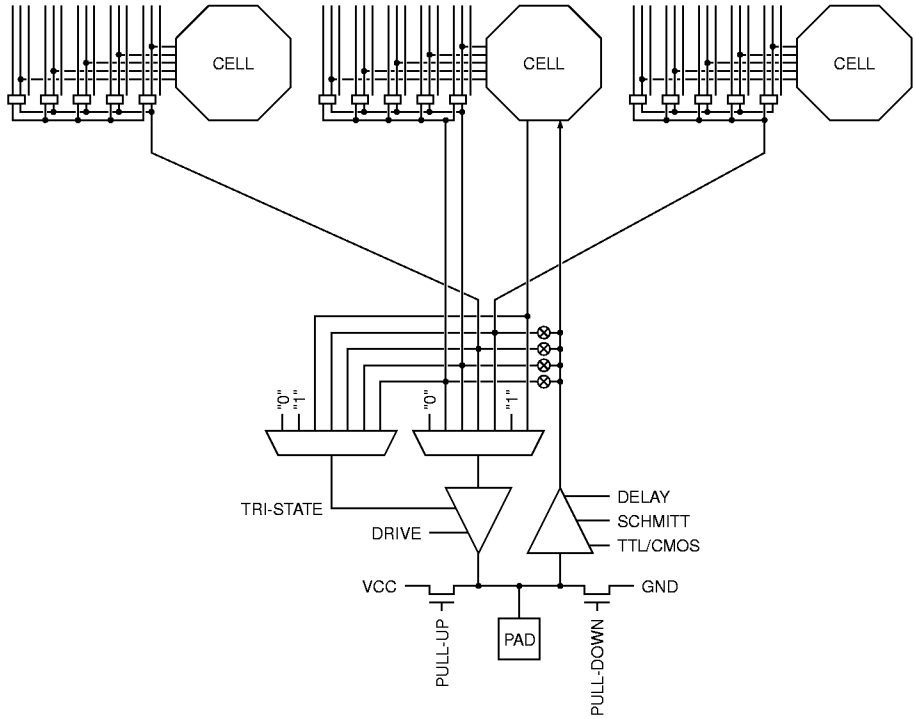


(a) Primary I/O

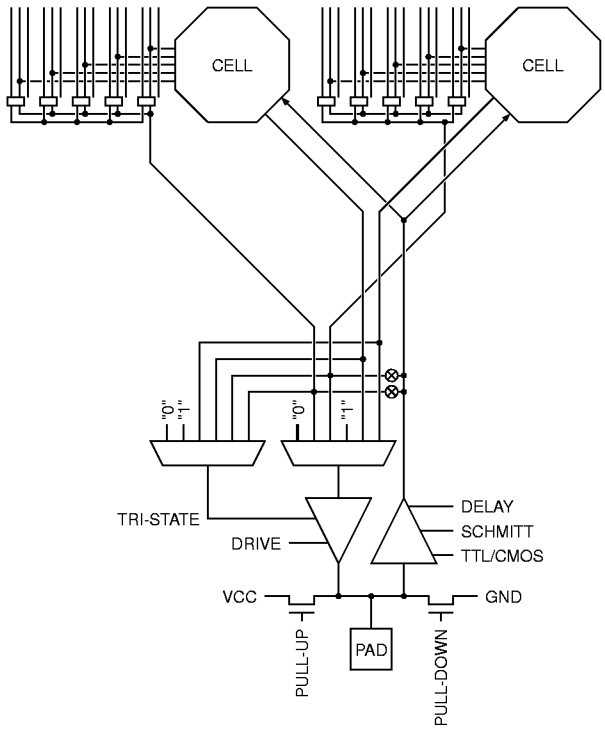


(a) Secondary I/O

Figure 13. South I/O (Mirrored for North I/O)

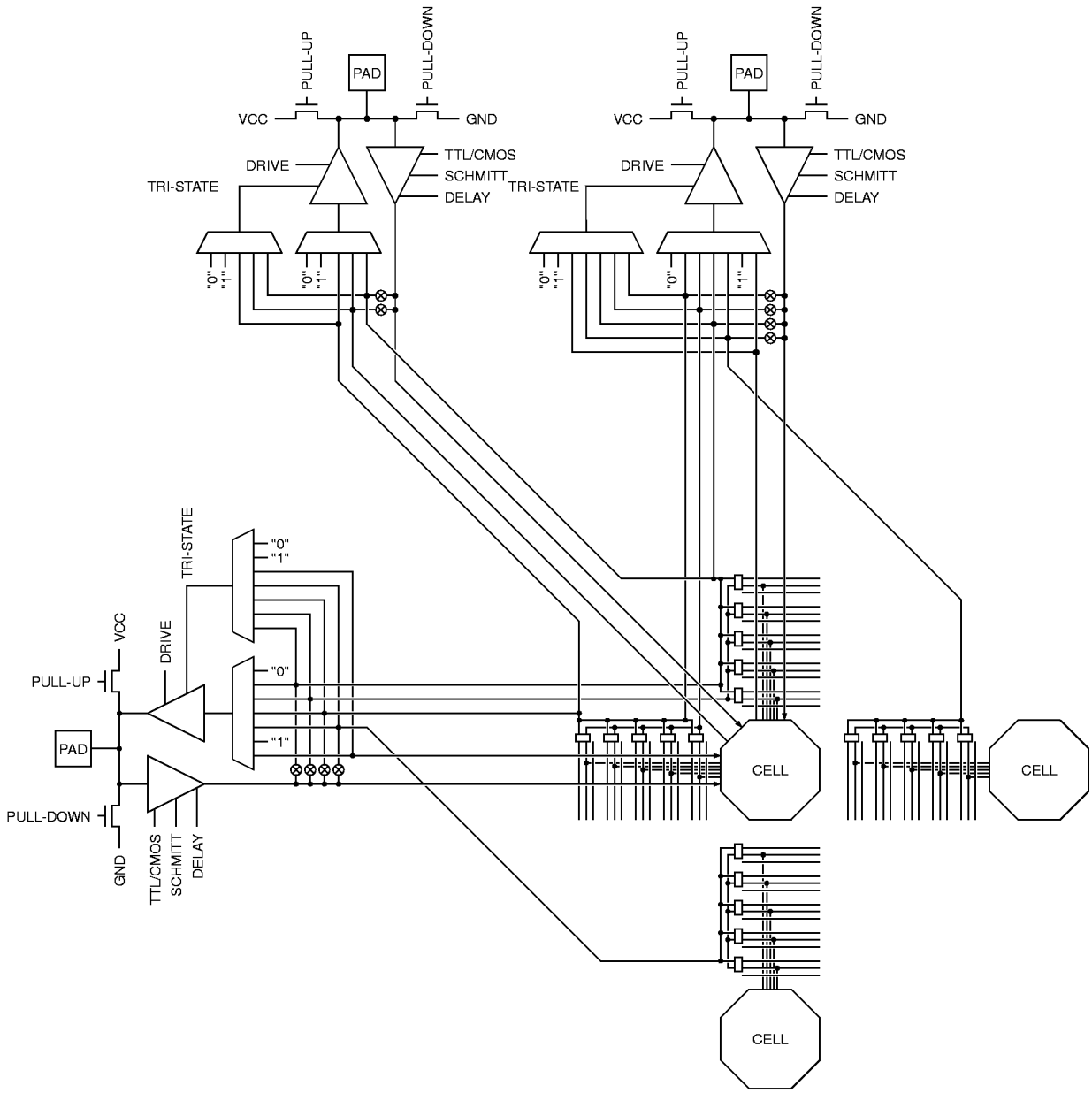


(a) Primary I/O



(a) Secondary I/O

Figure 14. North/West Corner, (similar for NE/SE/SW corners)



Some of the bus resource on ATK40K is used as a dual-function resource. Table 1 shows which buses are used in a dual-function mode and which bus plane is used. The ATK40K software tools are designed to accomodate dual-function buses in an efficient manner.

Table 1. Dual-Function Buses

Function	Type	Plane(s)	Direction	Comments
Cell Output Enable	Local	5	Horizontal and Vertical	
RAM Output Enable	Express	2	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Write Enable	Express	1	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Address	Express	1-5	Vertical	Buses full length at array edge Buses in second column to left of RAM block
RAM Data In	Local	1	Horizontal	
RAM Data Out	Local	2	Horizontal	
Clocking	Express	4	Vertical	Bus half length at array edge
Set/Reset	Express	5	Vertical	Bus half length at array edge

AC Timing Characteristics - 5V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.2V, temperature = 0°C
Max delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	-2.00	-1	Units
Core					
2 input gate	t_{PD}(max)	x/y -> x/y	1.68	1.34	ns
3 input gate	t_{PD}(max)	x/y/w -> x/y	2.62	2.10	ns
4 input gate	t_{PD}(max)	x/y/w/z -> x/y	2.62	2.10	ns
fast carry	t_{PD}(max)	y -> y	1.61	1.29	ns
fast carry	t_{PD}(max)	x -> y	1.78	1.42	ns
fast carry	t_{PD}(max)	y -> x	1.76	1.41	ns
fast carry	t_{PD}(max)	y -> y	1.64	1.31	ns
fast carry	t_{PD}(max)	w -> y	2.62	2.10	ns
fast carry	t_{PD}(max)	w -> x	2.62	2.10	ns
fast carry	t_{PD}(max)	z -> y	2.55	2.04	ns
fast carry	t_{PD}(max)	z -> x	2.53	2.02	ns
DFF	t_{PD}(max)	q -> x/y	2.40	1.92	ns
DFF	t_{setup}(min)	x/y -> clk	1.50	1.20	ns
DFF	t_{hold}(min)	x/y -> clk	0.00	0.00	ns
DFF	t_{PD}(max)	R -> x/y	2.70	2.16	ns
DFF	t_{PD}(max)	S -> x/y	2.95	2.36	ns
incremental FB	t_{PD}(max)	q -> w	0.30	0.24	ns
incremental --> L	t_{PD}(max)	x/y -> L	1.20	0.96	ns
Local output enable	t_{PZX}(max)	oe -> L	1.60	1.28	ns
Local output enable	t_{PXZ}(max)	oe -> L	1.80	1.44	ns

Cell Function	Parameter	Path	-2.00	-1	Units
Repeaters					
Repeater	t_{PD}(max)	L -> E	1.08	0.86	ns
Repeater	t_{PD}(max)	E -> E	1.08	0.86	ns
Repeater	t_{PD}(max)	L -> L	0.95	0.76	ns
Repeater	t_{PD}(max)	E -> L	0.95	0.76	ns
Repeater	t_{PD}(max)	E -> IO	0.80	0.64	ns
Repeater	t_{PD}(max)	L -> IO	0.80	0.64	ns

Notes:
1. TTL buffer delays are measured from a V_{IH} of 1.5V at the pad to the internal V_{IH} at A. The input buffer load is constant.
2. CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the pad to the internal V_{IH} at A. The input buffer load is constant.
3. Buffer delay is to a pad voltage of 1.5V with one output switching.
4. Parameter based on characterization and simulation; not tested in production.
5. Exact power calculation is available in an Atmel application note.

AC Timing Characteristics - 5V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.2V, temperature = 0°C
Max delays are the average of t_{PDLH} and t_{PDHL}.

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50 V_{DD}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

Cell Function	Parameter	Path	-2.00	-1	Units
IO					
Input	t_{PD}(max)	pad -> x/y	1.04	0.83	ns
Input	t_{PD}(max)	pad -> x/y	4.00	3.20	ns
Input	t_{PD}(max)	pad -> x/y	8.60	6.88	ns
Input	t_{PD}(max)	pad -> x/y	13.10	10.48	ns
Output, slow	t_{PD}(max)	x/y/E/L -> pad	6.30	5.04	ns
Output, medium	t_{PD}(max)	x/y/E/L -> pad	5.50	4.40	ns
Output, fast	t_{PD}(max)	x/y/E/L -> pad	4.50	3.60	ns
Output, slow	t_{PZX}(max)	oe -> pad	6.80	5.44	ns
Output, slow	t_{PXZ}(max)	oe -> pad	1.30	1.04	ns
Output, medium	t_{PZX}(max)	oe -> pad	5.70	4.56	ns
Output, medium	t_{PXZ}(max)	oe -> pad	1.85	1.48	ns
Output, fast	t_{PZX}(max)	oe -> pad	4.70	3.76	ns
Output, fast	t_{PXZ}(max)	oe -> pad	1.55	1.24	ns

Clocks and Reset Input buffers are measured from a V_{IH} of 1.5V at the input pad to the internal V_{IH} of 50% of V_{DD}.

Maximum times for clock input buffers and internal drivers are measured for rising edge delays only.

Cell Function	Parameter	Path	-2.00	-1	Units
Global Clocks and Set/Reset					
GCLK Input buffer	t_{PD}(max)	pad -> clock	2.60	2.08	ns
FCLK Input buffer	t_{PD}(max)	pad -> clock	0.80	0.64	ns
Clock column driver	t_{PD}(max)	clock -> colclk	1.30	1.04	ns
Clock sector driver	t_{PD}(max)	colclk -> secclk	0.75	0.60	ns
GSRN Input buffer	t_{PD}(max)	pad -> GSRN	5.60	4.48	ns

Notes:
1. TTL buffer delays are measured from a V_{IH} of 1.5V at the pad to the internal V_{IH} at A. The input buffer load is constant.
2. CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the pad to the internal V_{IH} at A. The input buffer load is constant.
3. Buffer delay is to a pad voltage of 1.5V with one output switching.
4. Parameter based on characterization and simulation; not tested in production.
5. Exact power calculation is available in an Atmel application note.

AC Timing Characteristics - 5V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.2V, temperature = 0°C
Max delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	-2.00	-1	Units
Async RAM					
Write	$t_{WECY}C$(min)	cycle time	8.00	8.00	ns
Write	t_{WEL}(min)	we	3.00	3.00	ns
Write	t_{WEH}(min)	we	3.00	3.00	ns
Write	t_{setup}(min)	wr addr setup-> we	2.00	2.00	ns
Write	t_{hold}(min)	wr addr hold -> we	0.00	0.00	ns
Write	t_{setup}(min)	din setup -> we	2.00	2.00	ns
Write	t_{hold}(min)	din hold -> we	0.00	0.00	ns
Write	t_{hold}(min)	oe hold -> we	0.00	0.00	ns
Write/Read	t_{PD}(max)	din -> dout	6.40	5.12	ns
Read	t_{PD}(max)	rd addr -> dout	3.60	2.88	ns
Read	t_{PZX}(max)	oe -> dout	2.90	2.32	ns
Read	t_{PXZ}(max)	oe -> dout	2.30	1.84	ns
Sync RAM					
Write	t_{CYC}(min)	cycle time	8.00	8.00	ns
Write	t_{CLKL}(min)	clk	3.00	3.00	ns
Write	t_{CLKH}(min)	clk	3.00	3.00	ns
Write	t_{setup}(min)	we setup-> clk	2.00	2.00	ns
Write	$t_{hold(}$min)	we hold -> clk	0.00	0.00	ns
Write	t_{setup}(min)	wr addr setup-> clk	2.00	2.00	ns
Write	t_{hold}(min)	wr addr hold -> clk	0.00	0.00	ns
Write	t_{setup}(min)	wr data setup-> clk	2.00	2.00	ns
Write	t_{hold}(min)	wr data hold -> clk	0.00	0.00	ns
Write/Read	t_{PD}(max)	din -> dout	6.40	5.12	ns
Write/Read	t_{PD}(max)	clk -> dout	5.10	4.08	ns
Read	t_{PD}(max)	rd addr -> dout	3.60	2.88	ns
Read	t_{PZX}(max)	oe -> dout	2.90	2.32	ns
Read	t_{PXZ}(max)	oe -> dout	2.30	1.84	ns

Notes:
1. TTL buffer delays are measured from a V_{IH} of 1.5V at the pad to the internal V_{IH} at A. The input buffer load is constant.
2. CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the pad to the internal V_{IH} at A. The input buffer load is constant.
3. Buffer delay is to a pad voltage of 1.5V with one output switching.
4. Parameter based on characterization and simulation; not tested in production.
5. Exact power calculation is available in an Atmel application note

AC Timing Characteristics - 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.2V, temperature = 0°C
Max delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	-2.00	-1	Units
Core					
2 input gate	t_{PD}(max)	x/y -> x/y			ns
3 input gate	t_{PD}(max)	x/y/w -> x/y			ns
4 input gate	t_{PD}(max)	x/y/w/z -> x/y			ns
fast carry	t_{PD}(max)	y -> y			ns
fast carry	t_{PD}(max)	x -> y			ns
fast carry	t_{PD}(max)	y -> x			ns
fast carry	t_{PD}(max)				ns
fast carry	t_{PD}(max)				ns
fast carry	t_{PD}(max)	w -> x			ns
fast carry	t_{PD}(max)	z -> w			ns
fast carry	t_{PD}(max)				ns
DFF	t_{PD}(max)	q -> x/y			ns
DFF	t_{setup}(min)	x/y -> clk			ns
DFF	t_{hold}(min)	x/y -> clk			ns
DFF	t_{PD}(max)	R -> x/y			ns
DFF	t_{PD}(max)	S -> x/y			ns
incremental FB	t_{PD}(max)	q -> w			ns
incremental --> L	t_{PD}(max)	x/y -> L			ns
Local output enable	t_{PZX}(max)	oe -> L			ns
Local output enable	t_{PXZ}(max)	oe -> L			ns

Cell Function	Parameter	Path	-2.00	-1	Units
Repeaters					
Repeater	t_{PD}(max)				ns
Repeater	t_{PD}(max)	E -> F			ns
Repeater	t_{PD}(max)				ns
Repeater	t_{PD}(max)	-> L			ns
Repeater	t_{PD}(max)				ns
Repeater	t_{PD}(max)	L -> IO			ns

Notes:
1. TTL buffer delays are measured from a V[illegible] 1.5V at the pad to the internal V_{IH} at A. The input buffer load is constant.
2. CMOS buffer delays are measured from a V[illegible] of 1/2 V_{CC} at the pad to the internal V_{IH} at A. The input buffer load is constant.
3. Buffer delay is to a pad voltage of 1.5V with one output switching.
4. Parameter based on characterization and simulation; not tested in production
5. Exact power calculation is available in an Atmel application note

AC Timing Characteristics - 3.3V Operation

Delays are based on fixed loads and are described in the notes.

Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C

Minimum times based on best case: V_{CC} = 5.2V, temperature = 0°C

Max delays are the average of t_{PDLH} and t_{PDHL}.

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50 V_{DD}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

Cell Function	Parameter	Path	-2.00	-1	Units
IO					
Input	t_{PD}(max)	pad -> x/y			ns
Input	t_{PD}(max)	pad -> x/y			ns
Input	t_{PD}(max)	pad -> x/y			ns
Input	t_{PD}(max)	[illegible]/y			ns
Output, slow	t_{PD}(max)	x/y/E/[illegible] -> pad			ns
Output, medium	t_{PD}(ma[illegible]	[illegible]			ns
Output, fast	[illegible]	[illegible]y/E/L -> [illegible]			ns
Output, slow	t_{PZX}(ma[illegible]	[illegible]			ns
Output, slow	t_{PXZ}(max)	o[illegible] -> pad			ns
Output, medium	t_{PZX}(max)	oe -> pad			ns
Output, medium	t_{PXZ}(max)	oe -> pad			ns
Output, fast	t_{PZX}(max)	oe -> pad			ns
Output, fast	t_{PXZ}(max)	oe -> pad			ns

Clocks and Reset Input buffers are measured from a V_{IH} of 1.5V at the input pad to the internal V_{IH} of 50% of V_{DD}.

Maxim[illegible]times for clock input buffers and internal drivers are m[illegible]for rising edge delays only.

Cell Function	Parameter	Path	-2.00	-1	Units
Global Clocks and Set/Reset					
GCLK Input buffer	t_{PD}[illegible]	pad -> [illegible]ck			ns
FCLK Input buffer	t_{PD}(m[illegible]	[illegible] -> [illegible]k			ns
Clock column driver	t_{PD}(ma[illegible]	[illegible]ck -> colclk			ns
Clock sector driver	t_{PD}(max)	colclk -> secclk			ns
GSRN Input buffer	t_{PD}(max)	pad -> GSRN			ns

Notes:
1. TTL buffer delays are measured from [illegible] of 1.5V at the pad to the internal V_{IH} at A. The input buffer load is constant.
2. CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the pad to the internal V_{IH} at A. The input buffer load is constant.
3. Buffer delay is to a pad voltage of 1.5V with one output switching.
4. Parameter based on characterization and simulation; not tested in production
5. Exact power calculation is available in an Atmel application note

AC Timing Characteristics - 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.2V, temperature = 0°C
Max delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	-2.00	-1	Units
Async RAM					
Write	$t_{WECY}C$(min)	cycle time			ns
Write	t_{WEL}(min)	we			ns
Write	t_{WEH}(min)	we			ns
Write	t_{setup}(min)	wr addr setup-> we			ns
Write	t_{hold}(min)	wr addr hold -> we			ns
Write	t_{setup}(min)	din setup -> we			ns
Write	t_{hold}(min)	din hold -> we			ns
Write	t_{hold}(min)	oe hold -> we			ns
Write/Read	t_{PD}(max)	din -> dout			ns
Read	t_{PD}(max)	rd addr -> dout			ns
Read	t_{PZX}(max)	oe -> dout			ns
Read	t_{PXZ}(max)	oe -> dout			ns
Sync RAM					
Write		cycle time			ns
Write	t_{CLKL}(min)	clk			ns
Write	t_{CLKH}(min)	clk			ns
Write	t_{setup}(min)	we setup-> clk			ns
Write	t_{hold}(min)	we hold -> clk			ns
Write	t_{setup}(min)	wr addr setup-> clk			ns
Write	t_{hold}(min)	wr addr hold -> clk			ns
Write	t_{setup}(min)	wr data setup-> clk			ns
Write	t_{hold}(min)	wr data hold -> clk			ns
Write/Read	t_{PD}(max)	din -> dout			ns
Write/Read	t_{PD}(max)	clk -> dout			ns
Read	t_{PD}(max)	rd addr -> dout			ns
Read	t_{PZX}(max)	oe -> dout			ns
Read	t_{PXZ}(max)	oe -> dout			ns

Notes:
1. TTL buffer delays are measured from a V_{IH} of 1.5V at the pad to the internal V_{IH} at A. The input buffer load is constant.
2. CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the pad to the internal V_{IH} at A. The input buffer load is constant.
3. Buffer delay is to a pad voltage of 1.5V with one output switching.
4. Parameter based on characterization and simulation; not tested in production
5. Exact power calculation is available in an Atmel application note

Absolute Maximum Rating*

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Voltage (V_{IN})	-0.5V to V_{CC} + 0.5V
DC Output Voltage (V_{ON})	-0.5V to V_{CC} + 0.5V
Storage Temperature Range (TSTG)	-65°C to +150°C
Power Dissipation (PD)	1500 mW
Lead Temperature (T_L) (Soldering, 10 sec.)	260°C
ESD (R_{ZAP}=1.5K, C_{ZAP}=100 pF)	2000V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range - 5V Operation

		AT40K05-2/1 AT40K10-2/1 AT40K20-2/1 AT40K30-2/1 AT40K40-2/1 Commercial	**AT40K05-2/1 AT40K10-2/1 AT40K20-2/1 AT40K30-2/1 AT40K40-2/1 Industrial**	**AT40K05-2 AT40K10-2 AT40K20-2 AT40K30-2 AT40K40-2 Military**
Operating Temperature (Case)		0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%
Input Voltage Level (TTL)	High (V_{IHT})	2.0V - V_{CC}	2.0V - V_{CC}	2.0V - V_{CC}
	Low (V_{ILT})	0V - 0.8V	0V - 0.8V	0V - 0.8V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}	70% - 100% V_{CC}	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}	0 - 30% V_{CC}	0 - 30% V_{CC}
Input Signal Transition Time	(T_{IN})	50 ns (max)	50 ns (max)	50 ns (max)

DC and AC Operating Range - 3.3V Operation

		AT40K05 AT40K10 AT40K20 AT40K30 AT40K40 Commercial
Operating Temperature (Case)		0°C - 70°C
V_{CC} Power Supply		3.3V ± 10%
Input Voltage Level (TTL)	High (V_{IHT})	2.0V - V_{CC}
	Low (V_{ILT})	0V - 0.8V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}
Input Signal Transition Time	(T_{IN})	50 ns (max)

DC Characteristics - 5V Operation

Symbol	Parameter	Conditions		Min	Max	Units
V_{IH}	High-Level Input Voltage	Commercial	CMOS	70% V_{CC}	V_{CC}	V
			TTL	2.0	V_{CC}	V
V_{IL}	Low-Level Input Voltage	Commercial	CMOS	0	30% V_{CC}	V
			TTL	0	0.8	V
V_{OH}	High-Level Output Voltage	Commercial	I_{OH} = -4 mA, V_{CC} min	3.9		V
			I_{OH} = -16 mA, V_{CC} min	3.0		V
V_{OL}	Low-Level Output Voltage	Commercial	I_{OL} = 4 mA, V_{CC} min		0.4	V
			I_{OL} = 16 mA, V_{CC} min		0.5	V
I_{OZH}	High-Level Tristate Output Leakage Current	V_O = V_{CC} (max)			10	µA
I_{OZL}	Low-Level Tristate Output Leakage Current	Without Pull-Up, V_O = V_{SS}		-10		µA
		With Pull-Up, V_O = V_{SS}		-500		µA
I_{IH}	High-Level Input Current	V_{IN} = V_{CC} (max)			10	µA
I_{IL}	Low-Level Input Current	Without Pull-Up, V_{IN} = V_{SS}		-10		µA
		With Pull-Up, V_{IN} = V_{SS}		-500		µA
I_{CC}	Power Consumption	Without Internal Oscillator (Standby)			500	µA
C_{IN}	Input Capacitance	All Pins			10	pF

DC Characteristics - 3.3V Operation

Symbol	Parameter	Conditions		Min	Max	Units
V_{IH}	High-Level Input Voltage	Commercial	CMOS	70% V_{CC}	V_{CC}	V
			TTL	2.0	V_{CC}	V
V_{IL}	Low-Level Input Voltage	Commercial	CMOS	0	30% V_{CC}	V
			TTL	0	0.8	V
V_{OH}	High-Level Output Voltage	Commercial	I_{OH} = -2mA, V_{CC} min	2.4		V
			I_{OH} = -6 mA, V_{CC} min	2.0		V
V_{OL}	Low-Level Output Voltage	Commercial	I_{OL} = +2 mA, V_{CC} min		0.4	V
			I_{OL} = +6 mA, V_{CC} min		0.5	V
I_{OZH}	High-Level Tristate Output Leakage Current	V_O = V_{CC} (max)			10	µA
I_{OZL}	Low-Level Tristate Output Leakage Current	Without Pull-Up, V_O = V_{SS}		-10		µA
		With Pull-Up, V_O = V_{SS}		-250		µA
I_{IH}	High-Level Input Current	V_{IN} = V_{CC} (max)			10	µA
I_{IL}	Low-Level Input Current	Without Pull-Up, V_{IN} = V_{SS}		-10		µA
		With Pull-Up, V_{IN} = V_{SS}		-250		µA
I_{CC}	Power Consumption	Without Internal Oscillator (Standby)			200	µA
C_{IN}[1]	Input Capacitance	All Pins			10	pF

Note: 1. Parameter based on characterization and simulation; it is not tested in production.

Part/Package Availability

	AT40K05	AT40K10	AT40K20	AT40K30	AT40K40
PC 84	X	X	X	X	X
TQ 100	X	X			
TQ 144	X	X	X	X	X
PQ 160	X	X	X	X	
PQ 208	X	X	X	X	X
PQ 240		X	X	X	X
PQ 304			X	X	X
BG 225		X	X	X	X
BG 352			X	X	X
BG 432				X	X
PG 475				X	X

USER I/O Counts - (Including Dual Function Pins)

	AT40K05	AT40K10	AT40K20	AT40K30	AT40K40
PC 84	61	61	61		
TQ 100	77	77			
TQ 144	113	113	113	113	
PQ 160	128	129	129	129	
PQ 208	128	160	160	160	160
PQ 240		192	193	193	193
PQ 304			256	256	256
BG 225		192	193	193	193
BG 352			256	256	256
BG 432				320	352
PG 475				320	384

Devices in same packages are pin-for-pin replaceable.

AT40K05	AT40K10	AT40K20	AT40K30	AT40K40	Left Side (Top to Bottom)										
128 I/O	192 I/O	256 I/O	320 I/O	384 I/O	PC 84	VQ 100	TQ 144	PQ 160	PQ 208	BG 225	PQ 240	PQ 304	BG 352	BG 432	PG475
GND	GND	GND	GND	GND	12	1	1	1	2	A1	1	304	GND*	GND*	GND*
I/O,,GCK1(A16)	I/O,GCK1(A16)	I/O,GCK1(A16)	I/O,GCK1(A16)	I/O,GCK1(A16)	13	2	2	2	4	D4	2	303	D23	D29	G7
I/O(A17)	I/O(A17)	I/O(A17)	I/O(A17)	I/O(A17)	14	3	3	3	5	B1	3	302	C25	C30	D4
I/O	I/O	I/O	I/O	I/O			4	4	6	C2	4	301	D24	E28	A5
I/O	I/O	I/O	I/O	I/O			5	5	7	E5	5	300	E23	E29	B4
I/O(A18)	I/O(A18)	I/O(A18)	I/O(A18)	I/O(A18)	15	4	6	6	8	D3	6	299	C26	D30	D6
I/O(A19)	I/O(A19)	I/O(A19)	I/O(A19)	I/O(A19)	16	5	7	7	9	C1	7	298	E24	D31	F8
				GND										GND*	GND*
				I/O										F28	B6
				I/O										F29	E7
			I/O	I/O										E30	D8
			I/O	I/O										E31	G9
		I/O	I/O	I/O								297	F24	G28	E9
		I/O	I/O	I/O								296	E25	G29	A7
		VCC	VCC	VCC									VCC*	VCC*	VCC*
		GND	GND	GND									GND*	GND*	GND*
			I/O	I/O										F30	B8
			I/O	I/O										F31	C9
I/O	I/O	I/O	I/O	I/O				8	10	D2	8	295	D26	H28	G11
I/O	I/O	I/O	I/O	I/O				9	11	G6	9	294	G24	H29	D10
	I/O	I/O	I/O	I/O					12	E4	10	293	F25	G30	E11
	I/O	I/O	I/O	I/O					13	D1	11	292	F26	H30	A9
				GND										GND*	GND*
				I/O											B10
				I/O											C11
	I/O	I/O	I/O	I/O						E3	12	291	H23	J28	F12
	I/O	I/O	I/O	I/O						E2	13	290	H24	J29	D12
		I/O	I/O	I/O								289	G25	H31	A11
		I/O	I/O	I/O								288	G26	J30	G15
GND	GND	GND	GND	GND			8	10	14	GND*	14	287	GND*	GND*	GND*
I/O,FCK1	I/O,FCK1	I/O,FCK1	I/O,FCK1	I/O,FCK1			9	11	15	F5	15	286	J23	K28	B12
I/O	I/O	I/O	I/O	I/O			10	12	16	E1	16	285	J24	K29	E13
I/O(A20)	I/O(A20)	I/O(A20)	I/O(A20)	I/O(A20)	17	6	11	13	17	F4	17	284	H25	K30	C13
I/O(A21)	I/O(A21)	I/O(A21)	I/O(A21)	I/O(A21)	18	7	12	14	18	F3	18	283	K23	K31	A13
	VCC	VCC	VCC	VCC						VCC*	19	282	VCC*	VCC*	VCC*
	I/O	I/O	I/O	I/O						F2	20	280	K24	L29	B14
	I/O	I/O	I/O	I/O						F1	21	279	J25	L30	C15
				GND										GND*	GND*
				I/O										M30	G17
				I/O										M28	F14
			I/O	I/O										M29	D16
			I/O	I/O										M31	D14
		I/O	I/O	I/O								278	L24	N31	A15
		I/O	I/O	I/O								277	K25	N28	C17
		GND‡	GND	GND							22		GND*	GND*	GND*
			VCC	VCC										VCC*	VCC*
			I/O	I/O										N29	D18
			I/O	I/O										N30	B18
		I/O	I/O	I/O								276	L25	P30	F16
		I/O	I/O	I/O								275	L26	P28	G19
	I/O	I/O	I/O	I/O					19	G4	23	274	M23	P29	E17
	I/O	I/O	I/O	I/O					20	G3	24	273	M24	R31	E19
				GND										GND*	GND*
I/O	I/O	I/O	I/O	I/O			13	15	21	G2	25	272	M25	R30	A19
I/O	I/O	I/O	I/O	I/O		8	14	16	22	G1	26	271	M26	R28	F18
				I/O											C19
				I/O											D20
I/O(A22)	I/O(A22)	I/O(A22)	I/O(A22)	I/O(A22)	19	9	15	17	23	G5	27	270	N24	R29	F20
I/O(A23)	I/O(A23)	I/O(A23)	I/O(A23)	I/O(A23)	20	10	16	18	24	H3	28	269	N25	T31	B20
GND	GND	GND	GND	GND	21	11	17	19	25	H2	29	268	GND*	GND*	GND*

AT40K05	AT40K10	AT40K20	AT40K30	AT40K40	Left Side (Top to Bottom)										
128 I/O	192 I/O	256 I/O	320 I/O	384 I/O	PC 84	VQ 100	TQ 144	PQ 160	PQ 208	BG 225	PQ 240	PQ 304	BG 352	BG 432	PG475
VCC	VCC	VCC	VCC	VCC	22	12	18	20	26	H1	30	267	VCC*	VCC*	VCC*
I/O	I/O	I/O	I/O	I/O	23	13	19	21	27	H4	31	266	N26	T30	C21
I/O	I/O	I/O	I/O	I/O	24	14	20	22	28	H5	32	265	P25	T29	A21
				I/O											D22
				I/O											B22
I/O	I/O	I/O	I/O	I/O		15	21	23	29	J2	33	264	P23	U31	E23
I/O	I/O	I/O	I/O	I/O			22	24	30	J1	34	263	P24	U30	F22
				GND										GND*	GND*
	I/O	I/O	I/O	I/O					31	J3	35	262	R26	U28	C23
	I/O	I/O	I/O	I/O					32	J4	36	261	R25	U29	F24
		I/O	I/O	I/O								260	R24	V30	A23
		I/O	I/O	I/O								259	R23	V29	E25
			I/O	I/O										V28	G23
			I/O	I/O										W31	B24
			VCC	VCC										VCC*	VCC*
		GND‡	GND	GND							37		GND*	GND*	GND*
		I/O	I/O	I/O								258	T26	W30	D24
		I/O	I/O	I/O								257	T25	W29	C25
				I/O										W28	D28
				I/O										Y31	A27
			I/O	I/O										Y30	E29
			I/O	I/O										Y29	C27
	I/O	I/O	I/O	I/O						J5	38	256	T23	Y28	G25
	I/O	I/O	I/O	I/O						K1	39	255	V26	AA30	D26
	VCC	VCC	VCC	VCC						VCC*	40	253	VCC*	VCC*	VCC*
I/O	I/O	I/O	I/O	I/O	25	16	23	25	33	K2	41	252	U24	AA29	F26
I/O	I/O	I/O	I/O	I/O	26	17	24	26	34	K3	42	251	V25	AB31	B28
I/O	I/O	I/O	I/O	I/O			25	27	35	J6	43	250	V24	AB30	D30
I/O,FCK2	I/O,FCK2	I/O,FCK2	I/O,FCK2	I/O,FCK2			26	28	36	L1	44	249	U23	AB29	A29
GND	GND	GND	GND	GND			27	29	37	GND*	45	248	GND*	GND*	GND*
		I/O	I/O	I/O								247	Y26	AB28	C29
		I/O	I/O	I/O								246	W25	AC30	G27
	I/O	I/O	I/O	I/O						L2	46	245	W24	AC29	F30
	I/O	I/O	I/O	I/O						K4	47	244	V23	AC28	B30
				I/O											E31
				I/O											C31
				GND										GND*	GND*
			I/O	I/O										AD31	F28
			I/O	I/O										AD30	D32
	I/O	I/O	I/O	I/O					38	L3	48	243	AA26	AD29	B32
	I/O	I/O	I/O	I/O					39	M1	49	242	Y25	AD28	G31
I/O	I/O	I/O	I/O	I/O				30	40	K5	50	241	Y24	AE30	A33
I/O	I/O	I/O	I/O	I/O				31	41	M2	51	240	AA25	AE29	C33
		GND	GND	GND									GND*	GND*	GND*
		VCC	VCC	VCC									VCC*	VCC*	VCC*
		I/O	I/O	I/O								239	AB25	AF31	B34
		I/O	I/O	I/O								238	AA24	AE28	A35
				I/O										AF30	E33
				I/O										AF29	D34
I/O	I/O	I/O	I/O	I/O	27	18	28	32	42	L4	52	237	Y23	AG31	D36
I/O	I/O	I/O	I/O	I/O		19	29	33	43	N1	53	236	AC26	AF28	B36
				GND										GND*	GND*
			I/O	I/O										AG30	F34
			I/O	I/O										AG29	D38
I/O	I/O	I/O	I/O	I/O			30	34	44	M3	54	235	AA23	AH31	C37
I/O	I/O	I/O	I/O	I/O			31	35	45	N2	55	234	AB24	AG28	G37
I/O(/OTS)	I/O(/OTS)	I/O(/OTS)	I/O(/OTS)	I/O(/OTS)	28	20	32	36	46	K6	56	233	AD25	AH30	B38
I/O,GCK2	I/O,GCK2	I/O,GCK2	I/O,GCK2	I/O,GCK2	29	21	33	37	47	P1	57	232	AC24	AJ30	F38
O(M1)	O(M1)	O(M1)	O(M1)	O(M1)	30	22	34	38	48	N3	58	231	AB23	AH29	A39
GND	GND	GND	GND	GND	31	23	35	39	49	GND*	59	230	GND*	GND*	GND*
I(M0)	I(M0)	I(M0)	I(M0)	I(M0)	32	24	36	40	50	P2	60	229	AD24	AH28	E35

AT40K05	AT40K10	AT40K20	AT40K30	AT40K40	Bottom Side (Left to Right)										
128 I/O	192 I/O	256 I/O	320 I/O	320 I/O	PC 84	VQ 100	TQ 144	PQ 160	PQ 208	BG 225	PQ 240	PQ 304	BG 352	BG 432	PG475
VCC	VCC	VCC	VCC	VCC	33	25	37	41	55	R1	61	228	VCC*	VCC*	VCC*
I(M2)	I(M2)	I(M2)	I(M2)	I(M2)	34	26	38	42	56	M4	62	227	AC23	AJ28	G33
I/O,GCK3	I/O,GCK3	I/O,GCK3	I/O,GCK3	I/O,GCK3	35	27	39	43	57	R2	63	226	AE24	AK29	J37
I/O(HDC)	I/O(HDC)	I/O(HDC)	I/O(HDC)	I/O(HDC)	36	28	40	44	58	P3	64	225	AD23	AH27	G35
I/O	I/O	I/O	I/O	I/O			41	45	59	L5	65	224	AC22	AK28	K36
I/O	I/O	I/O	I/O	I/O			42	46	60	N4	66	223	AF24	AJ27	C39
I/O	I/O	I/O	I/O	I/O		29	43	47	61	R3	67	222	AD22	AL28	K38
I/O(LDC)	I/O(LDC)	I/O(LDC)	I/O(LDC)	I/O(LDC)	37	30	44	48	62	P4	68	221	AE23	AH26	C41
				I/O										AK27	D40
				I/O										AJ26	L37
				GND											
			I/O	I/O										AL27	H36
			I/O	I/O										AH25	M36
		I/O	I/O	I/O								220	AE22	AK26	J35
		I/O	I/O	I/O								219	AF23	AL26	E41
		VCC	VCC	VCC									VCC*	VCC*	VCC*
		GND	GND	GND									GND*	GND*	GND*
I/O	I/O	I/O	I/O	I/O				49	63	K7	69	218	AD20	AH24	F40
I/O	I/O	I/O	I/O	I/O				50	64	M5	70	217	AE21	AJ25	H38
	I/O	I/O	I/O	I/O					65	R4	71	216	AF21	AK25	N37
	I/O	I/O	I/O	I/O					66	N5	72	215	AC19	AJ24	L35
			I/O	I/O										AH23	R35
			I/O	I/O										AK24	G41
				GND										GND*	GND*
				I/O											H40
				I/O											P38
	I/O	I/O	I/O	I/O						P5	73	214	AD19	AL24	J39
	I/O	I/O	I/O	I/O						L6	74	213	AE20	AH22	R37
		I/O	I/O	I/O								212	AF20	AJ23	J41
		I/O	I/O	I/O								211	AC18	AK23	K40
GND	GND	GND	GND	GND			45	51	67	GND*	75	210	GND*	GND*	GND*
I/O	I/O	I/O	I/O	I/O			46	52	68	R5	76	209	AD18	AJ22	L39
I/O	I/O	I/O	I/O	I/O			47	53	69	M6	77	208	AE19	AK22	M38
I/O	I/O	I/O	I/O	I/O	38	31	48	54	70	N6	78	207	AC17	AL22	T36
I/O	I/O	I/O	I/O	I/O	39	32	49	55	71	P6	79	206	AD17	AJ21	M40
	VCC	VCC	VCC	VCC						VCC*	80	204	VCC*	VCC*	VCC*
	I/O	I/O	I/O	I/O					72	R6	81	203	AE18	AH20	N39
	I/O	I/O	I/O	I/O					73	M7	82	202	AF18	AK21	N41
				GND										GND*	GND*
				I/O										AJ20	P40
				I/O										AH19	T38
			I/O	I/O										AK20	U35
			I/O	I/O										AJ19	U37
		I/O	I/O	I/O								201	AE17	AL20	R39
		I/O	I/O	I/O								200	AE16	AH18	R41
		GND‡	GND	GND							83		GND*	GND*	GND*
			VCC	VCC										VCC*	VCC*
		I/O	I/O	I/O								199	AF16	AK19	V36
		I/O	I/O	I/O								198	AC15	AJ18	U39
	I/O	I/O	I/O	I/O						N7	84	197	AD15	AL19	V38
	I/O	I/O	I/O	I/O						P7	85	196	AE15	AK18	V40
I/O	I/O	I/O	I/O	I/O		33	50	56	74	R7	86	195	AF15	AH17	W37
I/O	I/O	I/O	I/O	I/O		34	51	57	75	L7	87	194	AD14	AJ17	W35
				GND										GND*	GND*
				I/O											W41
				I/O											Y36
			I/O	I/O										AK17	W39
			I/O	I/O										AL17	AB36
I/O(D15)	I/O(D15)	I/O(D15)	I/O(D15)	I/O(D15)	40	35	52	58	76	N8	88	193	AE14	AJ16	Y40
I/O(INIT)	I/O(INIT)	I/O(INIT)	I/O(INIT)	I/O(INIT)	41	36	53	59	77	P8	89	192	AF14	AK16	Y38

AT40K05	AT40K10	AT40K20	AT40K30	AT40K40	Bottomt Side (Left to Right)										
128 I/O	192 I/O	256 I/O	320 I/O	384 I/O	PC 84	VQ 100	TQ 144	PQ 160	PQ 208	BG 225	PQ 240	PQ 304	BG 352	BG 432	PG475
VCC	VCC	VCC	VCC	VCC	42	37	54	60	78	R8	90	191	VCC*	VCC*	VCC*
GND	GND	GND	GND	GND	43	38	55	61	79	M8	91	190	GND*	GND*	GND*
I/O(D14)	I/O(D14)	I/O(D14)	I/O(D14)	I/O(D14)	44	39	56	62	80	L8	92	189	AE13	AL16	AA39
I/O(D13)	I/O(D13)	I/O(D13)	I/O(D13)	I/O(D13)	45	40	57	63	81	P9	93	188	AC13	AH15	AB38
			I/O	I/O										AL15	AB40
			I/O	I/O										AJ15	AC37
				I/O											AC39
				I/O											AC41
				GND										GND*	GND*
I/O	I/O	I/O	I/O	I/O		41	58	64	82	R9	94	187	AD13	AK15	AD36
I/O	I/O	I/O	I/O	I/O		42	59	65	83	N9	95	186	AF12	AJ14	AC35
	I/O	I/O	I/O	I/O					84	M9	96	185	AE12	AH14	AE37
	I/O	I/O	I/O	I/O					85	L9	97	184	AD12	AK14	AD40
		I/O	I/O	I/O								183	AC12	AL13	AD38
		I/O	I/O	I/O								182	AF11	AK13	AE39
			VCC	VCC										VCC*	VCC*
		GND‡	GND	GND							98		GND*	GND*	GND*
		I/O	I/O	I/O								181	AE11	AJ13	AG41
		I/O	I/O	I/O								180	AD11	AH13	AG39
			I/O	I/O										AL12	AG37
			I/O	I/O										AK12	AE35
				I/O										AJ12	AH38
				I/O										AK11	AF38
				GND										GND*	GND*
	I/O	I/O	I/O	I/O						R10	99	179	AF9	AH12	AF36
	I/O	I/O	I/O	I/O						P10	100	178	AD10	AJ11	AH40
	VCC	VCC	VCC	VCC						VCC*	101	177	VCC*	VCC*	VCC*
I/O(D12)	I/O(D12)	I/O(D12)	I/O(D12)	I/O(D12)	46	43	60	66	86	N10	102	175	AE9	AL10	AJ41
I/O(D11)	I/O(D11)	I/O(D11)	I/O(D11)	I/O(D11)	47	44	61	67	87	K9	103	174	AD9	AK10	AJ39
I/O	I/O	I/O	I/O	I/O			62	68	88	R11	104	173	AC10	AJ10	AJ37
I/O	I/O	I/O	I/O	I/O			63	69	89	P11	105	172	AF7	AK9	AG35
GND	GND	GND	GND	GND			64	70	90	GND*	106	171	GND*	GND*	GND*
		I/O	I/O	I/O								170	AE8	AL8	AK40
		I/O	I/O	I/O								169	AD8	AH10	AK38
	I/O	I/O	I/O	I/O						M10	107	168	AC9	AJ9	AL37
	I/O	I/O	I/O	I/O						N11	108	167	AF6	AK8	AL39
				I/O											AM38
				I/O											AM40
				GND										GND*	GND*
			I/O	I/O										AJ8	AN41
			I/O	I/O										AH9	AM36
	I/O	I/O	I/O	I/O					91	R12	109	166	AE7	AK7	AK36
	I/O	I/O	I/O	I/O					92	L10	110	165	AD7	AL6	AU41
I/O	I/O	I/O	I/O	I/O				71	93	P12	111	164	AE6	AJ7	AN39
I/O	I/O	I/O	I/O	I/O				72	94	M11	112	163	AE5	AH8	AP40
		GND	GND	GND									GND*	GND*	GND*
		VCC	VCC	VCC									VCC*	VCC*	VCC*
		I/O	I/O	I/O								162	AD6	AK6	AR41
		I/O	I/O	I/O								161	AC7	AL5	AL35
I/O(D10)	I/O(D10)	I/O(D10)	I/O(D10)	I/O(D10)	48	45	65	73	95	R13	113	160	AF4	AH7	AV40
I/O(D9)	I/O(D9)	I/O(D9)	I/O(D9)	I/O(D9)	49	46	66	74	96	N12	114	159	AF3	AJ6	AN37
			I/O	I/O										AK5	AT38
			I/O	I/O										AL4	AP38
				GND										GND*	GND*
				I/O										AH6	AT40
				I/O										AJ5	AW39
I/O	I/O	I/O	I/O	I/O			67	75	97	P13	115	158	AD5	AK4	AP36
I/O	I/O	I/O	I/O	I/O			68	76	98	K10	116	157	AE3	AH5	AU37
I/O(D8)	I/O(D8)	I/O(D8)	I/O(D8)	I/O(D8)	50	47	69	77	99	R14	117	156	AD4	AK3	AR37
I/O,GCK4	I/O,GCK4	I/O,GCK4	I/O,GCK4	I/O,GCK4	51	48	70	78	100	N13	118	155	AC5	AJ4	AU39
GND	GND	GND	GND	GND	52	49	71	79	101	GND*	119	154	GND*	GND*	GND*
/CON	/CON	/CON	/CON	/CON	53	50	72	80	103	P14	120	153	AD3	AH4	AR35

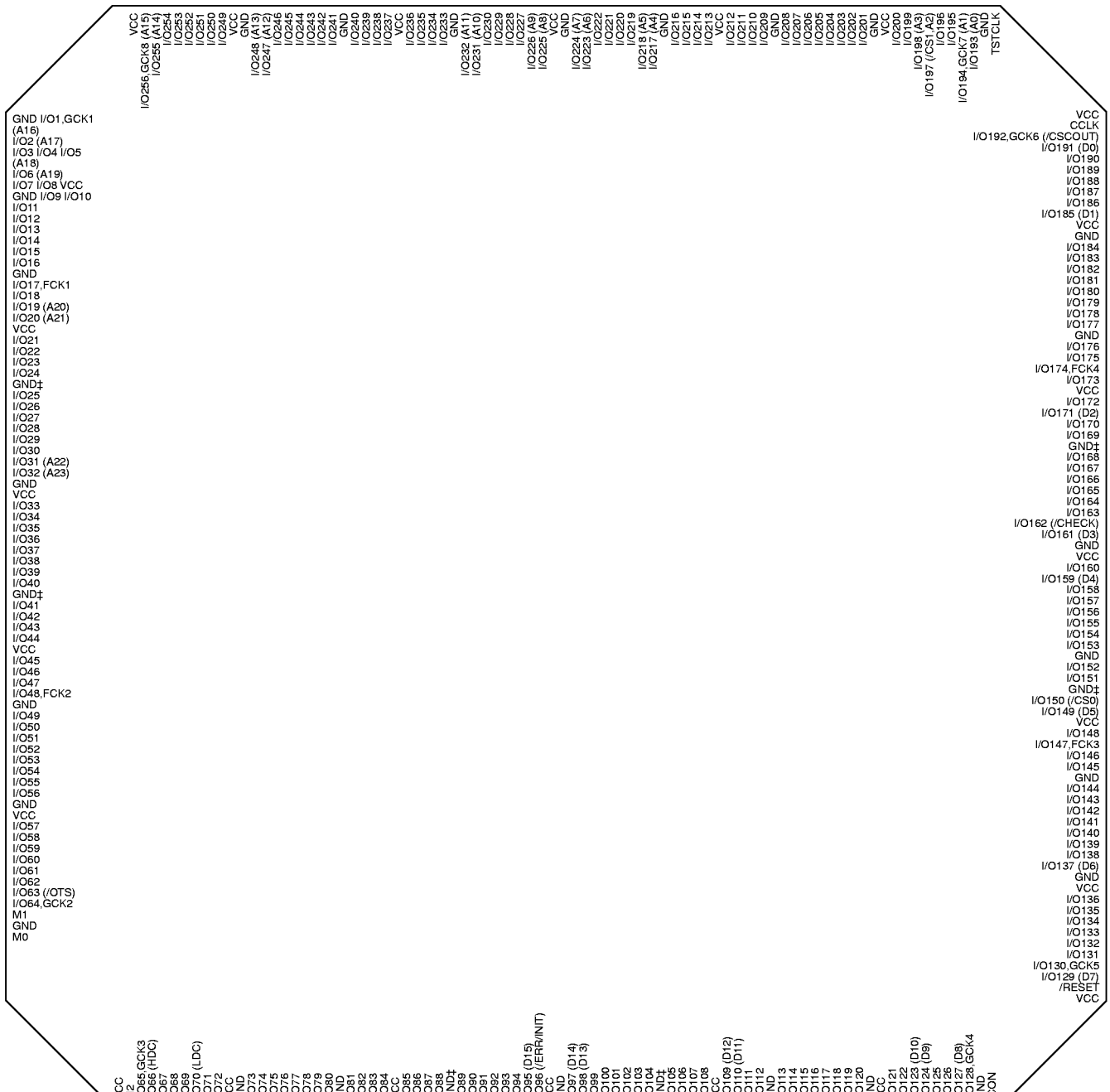
AT40K05	AT40K10	AT40K20	AT40K30	AT40K40	Right Side (Bottom to Top)										
128 I/O	192 I/O	256 I/O	320 I/O	320 I/O	PC 84	VQ 100	TQ 144	PQ 160	PQ 208	BG 225	PQ 240	PQ 304	BG 352	BG 432	PG475
VCC	VCC	VCC	VCC	VCC	54	51	73	81	106	R15	121	152	VCC*	VCC*	VCC*
/RESET	/RESET	/RESET	/RESET	/RESET	55	52	74	82	108	M12	122	151	AC4	AH3	AN35
I/O(D7)	I/O(D7)	I/O(D7)	I/O(D7)	I/O(D7)	56	53	75	83	109	P15	123	150	AD2	AJ2	AU35
I/O,GCK5	I/O,GCK5	I/O,GCK5	I/O,GCK5	I/O,GCK5	57	54	76	84	110	N14	124	149	AC3	AG4	AV38
I/O	I/O	I/O	I/O	I/O			77	85	111	L11	125	148	AB4	AG3	AT34
I/O	I/O	I/O	I/O	I/O			78	86	112	M13	126	147	AD1	AH2	BA39
			I/O	I/O										AH1	AU33
			I/O	I/O										AF4	AY38
				GND										GND*	GND*
	I/O	I/O	I/O	I/O						N15	127	146	AA4	AF3	AV36
	I/O	I/O	I/O	I/O						M14	128	145	AA3	AG2	AR31
				I/O										AG1	AR33
				I/O										AE4	AV32
		I/O	I/O	I/O								144	AB2	AE3	BA37
		I/O	I/O	I/O								143	AC1	AF2	AY36
		VCC	VCC	VCC									VCC*	VCC*	VCC*
		GND	GND	GND									GND*	GND*	GND*
I/O(D6)	I/O(D6)	I/O(D6)	I/O(D6)	I/O(D6)	58	55	79	87	113	J10	129	142	Y3	AF1	AV34
I/O	I/O	I/O	I/O	I/O		56	80	88	114	L12	130	141	AA2	AD4	BA35
I/O	I/O	I/O	I/O	I/O				89	115	M15	131	140	AA1	AD3	AU31
I/O	I/O	I/O	I/O	I/O				90	116	L13	132	139	W4	AE2	AY34
			I/O	I/O										AD2	AT30
			I/O	I/O										AC4	AW33
				GND										GND*	GND*
				I/O											BA33
				I/O											AV30
	I/O	I/O	I/O	I/O					117	L14	133	138	W3	AC3	AY32
	I/O	I/O	I/O	I/O					118	K11	134	137	Y2	AD1	AU29
		I/O	I/O	I/O								136	Y1	AC2	AW31
		I/O	I/O	I/O								135	V4	AB4	BA31
GND	GND	GND	GND	GND			81	91	119	GND*	135	134	GND*	GND*	GND*
	I/O	I/O	I/O	I/O						L15	136	133	V3	AB3	AR27
	I/O	I/O	I/O	I/O						K12	137	132	W2	AB2	AT28
I/O,FCK3	I/O,FCK3	I/O,FCK3	I/O,FCK3	I/O,FCK3			82	92	120	K13	138	131	U4	AB1	AY30
I/O	I/O	I/O	I/O	I/O			83	93	121	K14	139	130	U3	AA3	AW29
	VCC	VCC	VCC	VCC						VCC*	140	129	VCC*	VCC*	VCC*
I/O(D5)	I/O(D5)	I/O(D5)	I/O(D5)	I/O(D5)	59	57	84	94	122	K15	141	127	V2	AA2	BA29
I/O(CS0)	I/O(CS0)	I/O(CS0)	I/O(CS0)	I/O(CS0)	60	58	85	95	123	J12	142	126	V1	Y2	AY28
		GND‡		GND							143			GND*	GND*
			I/O	I/O										Y4	AR25
			I/O	I/O										Y3	AV28
				I/O										Y1	AW27
				I/O										W1	AT26
		I/O	I/O	I/O								125	U2	W4	AV26
		I/O	I/O	I/O								124	T2	W3	BA27
		GND	GND	GND									GND*	GND*	GND*
			VCC	VCC										VCC*	VCC*
			I/O	I/O										W2	AW25
			I/O	I/O										V2	AV24
		I/O	I/O	I/O								123	T1	V4	AU25
		I/O	I/O	I/O								122	R4	V3	AR23
	I/O	I/O	I/O	I/O					124	J13	144	121	R3	U1	AT24
	I/O	I/O	I/O	I/O					125	J14	145	120	R2	U2	AY24
				GND										GND*	GND*
I/O	I/O	I/O	I/O	I/O		59	86	96	126	J15	146	119	R1	U4	BA23
I/O	I/O	I/O	I/O	I/O		60	87	97	127	J11	147	118	P3	U3	AU23
				I/O											AW23
				I/O											AV20
I/O(D4)	I/O(D4)	I/O(D4)	I/O(D4)	I/O(D4)	61	61	88	98	128	H13	148	117	P2	T1	AY22
I/O	I/O	I/O	I/O	I/O	62	62	89	99	129	H14	149	116	P1	T2	AV22
VCC	VCC	VCC	VCC	VCC	63	63	90	100	130	H15	150	115	VCC*	VCC*	VCC*

AT40K05	AT40K10	AT40K20	AT40K30	AT40K40	Right Side (Bottom to Top)										
128 I/O	192 I/O	256 I/O	320 I/O	384 I/O	PC 84	VQ 100	TQ 144	PQ 160	PQ 208	BG 225	PQ 240	PQ 304	BG 352	BG 432	PG475
GND	GND	GND	GND	GND	64	64	91	101	131	GND*	151	114	GND*	GND*	GND*
I/O(D3)	I/O(D3)	I/O(D3)	I/O(D3)	I/O(D3)	65	65	92	102	132	H12	152	113	N2	T3	AW21
I/O(/CHECK)	I/O(/CHECK)	I/O(/CHECK)	I/O(/CHECK)	I/O(/CHECK)	66	66	93	103	133	H11	153	112	N4	R1	BA21
				I/O											AU19
				I/O											AY20
I/O	I/O	I/O	I/O	I/O		67	94	104	134	G14	154	111	N3	R2	AU17
I/O	I/O	I/O	I/O	I/O			95	105	135	G15	155	110	M1	R4	AW19
				GND										GND*	GND*
	I/O	I/O	I/O	I/O					136	G13	156	109	M2	R3	BA19
	I/O	I/O	I/O	I/O					137	G12	157	108	M3	P2	AT16
		I/O	I/O	I/O								107	M4	P3	AR19
		I/O	I/O	I/O								106	L1	P4	AV14
			I/O	I/O										N1	AY18
			I/O	I/O										N2	AV18
			VCC	VCC										VCC*	VCC*
		GND‡	GND	GND							158		GND*	GND*	GND*
		I/O	I/O	I/O								105	L2	N3	AT18
		I/O	I/O	I/O								104	L3	N4	AW17
			I/O	I/O										M1	AR15
			I/O	I/O										M2	BA15
				I/O										M3	AT14
				I/O										M4	AR17
				GND										GND*	GND*
I/O(D2)	I/O(D2)	I/O(D2)	I/O(D2)	I/O(D2)	67	68	96	106	138	G11	159	103	J1	L2	AW15
I/O	I/O	I/O	I/O	I/O	68	69	97	107	139	F15	160	102	K3	L3	AV16
	VCC	VCC	VCC	VCC						VCC*	161	101	VCC*	VCC*	VCC*
I/O	I/O	I/O	I/O	I/O			98	108	140	F14	162	99	J2	K1	AY14
I/O,FCK4	I/O,FCK4	I/O,FCK4	I/O,FCK4	I/O,FCK4			99	109	141	F13	163	98	J3	K2	BA13
	I/O	I/O	I/O	I/O						G10	164	97	K4	K3	AU13
	I/O	I/O	I/O	I/O						E15	165	96	G1	K4	AW13
GND	GND	GND	GND	GND			100	110	142	GND*	166	95	GND*	GND*	GND*
		I/O	I/O	I/O								94	H2	J2	AY12
		I/O	I/O	I/O								93	H3	J3	BA11
	I/O	I/O	I/O	I/O						E14	167	92	J4	J4	AV12
	I/O	I/O	I/O	I/O						F12	168	91	F1	H1	AT12
				I/O											AW11
				I/O											AY10
				GND										GND*	GND*
	I/O	I/O	I/O	I/O					143	E13	169	90	G2	H2	BA9
	I/O	I/O	I/O	I/O					144	D15	170	89	G3	H3	AU11
I/O	I/O	I/O	I/O	I/O				111	145	F11	171	88	F2	H4	AW9
I/O	I/O	I/O	I/O	I/O				112	146	D14	172	87	E2	G2	AV10
			I/O	I/O										G3	AY8
			I/O	I/O										F1	BA7
		GND	GND	GND									GND*	GND*	GND*
		VCC	VCC	VCC									VCC*	VCC*	VCC*
I/O(D1)	I/O(D1)	I/O(D1)	I/O(D1)	I/O(D1)	69	70	101	113	147	E12	173	86	F3	G4	AV8
I/O	I/O	I/O	I/O	I/O	70	71	102	114	148	C15	174	85	G4	F2	AY6
			I/O	I/O										F3	AR11
			I/O	I/O										E1	AT8
				I/O										F4	AU9
				I/O										E2	AW5
				GND										GND*	GND*
		I/O	I/O	I/O								84	D2	E3	AY4
		I/O	I/O	I/O								83	F4	D1	BA5
I/O	I/O	I/O	I/O	I/O			103	115	149	D13	175	82	E3	E4	AV4
I/O	I/O	I/O	I/O	I/O			104	116	150	C14	176	81	C2	D2	AR9
I/O(D0)	I/O(D0)	I/O(D0)	I/O(D0)	I/O(D0)	71	72	105	117	151	F10	177	80	D3	C2	AU5
I/O,GCK6(/CSOUT)	I/O,GCK6(/CSOUT)	I/O,GCK6(/CSOUT)	I/O,GCK6(/CSOUT)	I/O,GCK6(/CSOUT)	72	73	106	118	152	B15	178	79	E4	D3	AV6
CCLK	CCLK	CCLK	CCLK	CCLK	73	74	107	119	153	C13	179	78	C3	D4	AR5
VCC	VCC	VCC	VCC	VCC	74	75	108	120	154	B14	180	77	VCC*	VCC*	VCC*

AT40K05	AT40K10	AT40K20	AT40K30	AT40K40	Top Side (Right to Left)										
128 I/O	192 I/O	256 I/O	320 I/O	320 I/O	PC 84	VQ 100	TQ 144	PQ 160	PQ 208	BG 225	PQ 240	PQ 304	BG 352	BG 432	PG475
TSTCLK	TSTCLK	TSTCLK	TSTCLK	TSTCLK	75	76	109	121	159	A15	181	76	D4	C4	AN7
GND	GND	GND	GND	GND	76	77	110	122	160	D12	182	75	GND*	GND*	GND*
I/O(A0)	I/O(A0)	I/O(A0)	I/O(A0)	I/O(A0)	77	78	111	123	161	A14	183	74	B3	B3	AR7
I/O,GCK7(A1)	I/O,GCK7(A1)	I/O,GCK7(A1)	I/O,GCK7(A1)	I/O,GCK7(A1)	78	79	112	124	162	B13	184	73	C4	D5	AW3
I/O	I/O	I/O	I/O	I/O			113	125	163	E11	185	72	D5	B4	AU3
I/O	I/O	I/O	I/O	I/O			114	126	164	C12	186	71	A3	C5	AW1
				I/O										A4	AP6
				I/O										D6	AV2
				GND										GND*	GND*
			I/O	I/O										B5	AT4
			I/O	I/O										C6	AN5
I/O(/CS1,A2)	I/O(/CS1,A2)	I/O(/CS1,A2)	I/O(/CS1,A2)	I/O(/CS1,A2)	79	80	115	127	165	A13	187	70	D6	A5	AU1
I/O(A3)	I/O(A3)	I/O(A3)	I/O(A3)	I/O(A3)	80	81	116	128	166	B12	188	69	C6	D7	AM6
		I/O	I/O	I/O								68	B5	B6	AT2
		I/O	I/O	I/O								67	A4	A6	AL7
		VCC	VCC	VCC									VCC*	VCC*	VCC*
		GND	GND	GND									GND*	GND*	GND*
	I/O	I/O	I/O	I/O						F9	189	66	C7	D8	AR1
	I/O	I/O	I/O	I/O						D11	190	65	B6	C7	AP2
I/O	I/O	I/O	I/O	I/O			117	129	167	A12	191	64	A6	B7	AM4
I/O	I/O	I/O	I/O	I/O				130	168	C11	192	63	D8	D9	AN3
			I/O	I/O										B8	AL5
			I/O	I/O										A8	AK6
				GND										GND*	GND*
				I/O											AN1
				I/O											AJ5
	I/O	I/O	I/O	I/O					169	B11	193	62	B7	D10	AM2
	I/O	I/O	I/O	I/O					170	E10	194	61	A7	C9	AH4
		I/O	I/O	I/O							195	60	D9	B9	AL3
		I/O	I/O	I/O								59	C9	C10	AK4
GND	GND	GND	GND	GND			118	131	171	GND*	196	58	GND*	GND*	GND*
I/O	I/O	I/O	I/O	I/O			119	132	172	A11	197	57	B8	B10	AG7
I/O	I/O	I/O	I/O	I/O			120	133	173	D10	198	56	D10	A10	AG5
	I/O	I/O	I/O	I/O						C10	199	55	C10	C11	AK2
	I/O	I/O	I/O	I/O						B10	200	54	B9	D12	AJ3
	VCC	VCC	VCC	VCC						VCC*	201	52	VCC*	VCC*	VCC*
		I/O	I/O	I/O								51	A9	B11	AJ1
		I/O	I/O	I/O								50	D11	C12	AF6
				GND										GND*	GND*
				I/O										D13	AH2
				I/O										B12	AF4
			I/O	I/O										C13	AE7
			I/O	I/O										A12	AE5
		I/O	I/O	I/O								49	B11	D14	AG3
		I/O	I/O	I/O								48	A11	B13	AG1
		GND	GND	GND									GND*	GND*	GND*
			VCC	VCC										VCC*	VCC*
I/O(A4)	I/O(A4)	I/O(A4)	I/O(A4)	I/O(A4)	81	82	121	134	174	A10	202	47	D12	C14	AD6
I/O(A5)	I/O(A5)	I/O(A5)	I/O(A5)	I/O(A5)	82	83	122	135	175	D9	203	46	C12	A13	AD4
				GND							204				
	I/O	I/O	I/O	I/O					176	C9	205	45	B12	B14	AE3
	I/O	I/O	I/O	I/O				136	177	B9	206	44	A12	D15	AC5
I/O	I/O	I/O	I/O	I/O		84	123	137	178	A9	207	43	C13	C15	AD2
I/O	I/O	I/O	I/O	I/O		85	124	138	179	E9	208	42	B13	B15	AC7
				GND										GND*	GND*
				I/O											AC1
				I/O											AC3
			I/O	I/O										A15	AB6
			I/O	I/O										C16	AB2
I/O(A6)	I/O(A6)	I/O(A6)	I/O(A6)	I/O(A6)	83	86	125	139	180	C8	209	41	A13	B16	AB4
I/O(A7)	I/O(A7)	I/O(A7)	I/O(A7)	I/O(A7)	84	87	126	140	181	B8	210	40	B14	A16	AA3

AT40K05	AT40K10	AT40K20	AT40K30	AT40K40	Top Side (Right to Left)										
128 I/O	192 I/O	256 I/O	320 I/O	384 I/O	PC 84	VQ 100	TQ 144	PQ 160	PQ 208	BG 225	PQ 240	PQ 304	BG 352	BG 432	PG475
GND	GND	GND	GND	GND	1	88	127	141	182	A8	211	39	GND*	GND*	GND*
VCC	VCC	VCC	VCC	VCC	2	89	128	142	183	D8	212	38	VCC*	VCC*	VCC*
I/O(A8)	I/O(A8)	I/O(A8)	I/O(A8)	I/O(A8)	3	90	129	143	184	E8	213	37	D14	D17	Y2
I/O(A9)	I/O(A9)	I/O(A9)	I/O(A9)	I/O(A9)	4	91	130	144	185	B7	214	36	C14	A17	Y4
			I/O	I/O										C17	W5
			I/O	I/O										B17	Y6
				I/O											U3
				I/O											W3
														GND*	GND*
I/O	I/O	I/O	I/O	I/O		92	131	145	186	A7	215	35	A15	C18	W1
I/O	I/O	I/O	I/O	I/O		93	132	146	187	C7	216	34	B15	D18	U5
	I/O	I/O	I/O	I/O					188	D7	217	33	C15	B18	W7
	I/O	I/O	I/O	I/O					189	E7	218	32	D15	A19	U7
				GND							219				
I/O(A10)	I/O(A10)	I/O(A10)	I/O(A10)	I/O(A10)	5	94	133	147	190	A6	220	31	A16	B19	V2
I/O(A11)	I/O(A11)	I/O(A11)	I/O(A11)	I/O(A11)	6	95	134	148	191	B6	221	30	B16	C19	V4
			VCC	VCC										VCC*	VCC*
		GND	GND	GND									GND*	GND*	GND*
		I/O	I/O	I/O								29	C16	D19	V6
		I/O	I/O	I/O								28	B17	A20	R1
			I/O	I/O										B20	T6
			I/O	I/O										C20	R3
				I/O										B21	R5
				I/O										D20	T4
				GND										GND*	GND*
		I/O	I/O	I/O								27	C17	C21	P2
		I/O	I/O	I/O								26	B18	A22	N1
	VCC	VCC	VCC	VCC						VCC*	222	25	VCC*	VCC*	VCC*
	I/O	I/O	I/O	I/O						C6	223	23	C18	B22	N3
	I/O	I/O	I/O	I/O						F7	224	22	D17	C22	P4
I/O	I/O	I/O	I/O	I/O			135	149	192	A5	225	21	A20	B23	R7
I/O	I/O	I/O	I/O	I/O			136	150	193	B5	226	20	B19	A24	M2
GND	GND	GND	GND	GND			137	151	194	GND*	227	19	GND*	GND*	GND*
		I/O	I/O	I/O								18	C19	D22	M4
		I/O	I/O	I/O								17	D18	C23	L3
	I/O	I/O	I/O	I/O					195	D6	228	16	A21	B24	N5
	I/O	I/O	I/O	I/O					196	C5	229	15	B20	C24	K2
				I/O											L5
				I/O											J1
				GND										GND*	GND*
			I/O	I/O										D23	M6
			I/O	I/O										B25	K4
I/O	I/O	I/O	I/O	I/O				152	197	A4	230	14	C20	A26	J3
I/O	I/O	I/O	I/O	I/O				153	198	E6	231	13	B21	C25	J5
I/O(A12)	I/O(A12)	I/O(A12)	I/O(A12)	I/O(A12)	7	96	138	154	199	B4	232	12	B22	D24	H2
I/O(A13)	I/O(A13)	I/O(A13)	I/O(A13)	I/O(A13)	8	97	139	155	200	D5	233	10	C21	B26	G1
		GND	GND	GND									GND*	GND*	GND*
		VCC	VCC	VCC									VCC*	VCC*	VCC*
		I/O	I/O	I/O								9	D20	A27	L7
		I/O	I/O	I/O								8	A23	D25	K6
			I/O	I/O										C26	E1
			I/O	I/O										B27	H4
				I/O										A28	G5
				I/O										D26	F2
				GND										GND*	GND*
	I/O	I/O	I/O	I/O						A3	234	7	D21	C27	H6
	I/O	I/O	I/O	I/O						C4	235	6	C22	B28	C3
I/O	I/O	I/O	I/O	I/O			140	156	201	B3	236	5	B24	D27	F4
I/O	I/O	I/O	I/O	I/O			141	157	202	F6	237	4	C23	B29	C5
I/O(A14)	I/O(A14)	I/O(A14)	I/O(A14)	I/O(A14)	9	98	142	158	203	A2	238	3	D22	C28	E3
I/O,GCK8(A15)	I/O,GCK8(A15)	I/O,GCK8(A15)	I/O,GCK8(A15)	I/O,GCK8(A15)	10	99	143	159	204	C3	239	2	C24	D28	E5
VCC	VCC	VCC	VCC	VCC	11	100	144	160	205	B2	240	1	VCC*	VCC*	VCC*

Figure 15. AT40K20 Pad Ring



Ordering Information

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
5,000-10,000	1	AT40K05-1AJC AT40K05-1AQC AT40K05-1BQC AT40K05-1DQC	84J 100Q 144Q 208Q	5V Commercial (0°C to 70°C)
5,000-10,000	1	AT40K05-1AJI AT40K05-1AQI AT40K05-1BQI AT40K05-1DQI	84J 100Q 144Q 208Q	5V Industrial (-40°C to 85°C)
5,000-10,000	1	AT40K05LV-1AJC AT40K05LV-1AQC AT40K05LV-1BQC AT40K05LV-1DQC	84J 100Q 144Q 208Q	3.3V Commercial (0°C to 70°C)
5,000-10,000	1	AT40K05LV-1AJI AT40K05LV-1AQI AT40K05LV-1BQI AT40K05LV-1DQI	84J 100Q 144Q 208Q	3.3V Industrial (0°C to 70°C)

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
10,000-20,000	1	AT40K10-1AJC AT40K10-1AQC AT40K10-1BQC AT40K10-1DQC AT40K10-1EQC	84J 100Q 144Q 208Q 240Q	5V Commercial (0°C to 70°C)
10,000-20,000	1	AT40K10-1AJI AT40K10-1AQI AT40K10-1BQI AT40K10-1DQI AT40K10-1EQI	84J 100Q 144Q 208Q 240Q	5V Industrial (-40°C to 85°C)
10,000-20,000	1	AT40K10LV-1AJC AT40K10LV-1AQC AT40K10LV-1BQC AT40K10LV-1DQC AT40K10LV-1EQC	84J 100Q 144Q 208Q 240Q	3.3V Commercial (0°C to 70°C)
10,000-20,000	1	AT40K10LV-1AJI AT40K10LV-1AQI AT40K10LV-1BQI AT40K10LV-1DQI AT40K10LV-1EQI	84J 100Q 144Q 208Q 240Q	3.3V Industrial (-40°C to 85°C)

Ordering Information

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
20,000-30,000	1	AT40K20-1AJC AT40K20-1BQC AT40K20-1DQC AT40K20-1EQC AT40K20-1FQC AT40K20-1BGC	84J 144Q 208Q 240Q 304Q 352G	5V Commercial (0°C to 70°C)
20,000-30,000	1	AT40K20-1AJI AT40K20-1BQI AT40K20-1DQI AT40K20-1EQI AT40K20-1FQI AT40K20-1BGI	84J 144Q 208Q 240Q 304Q 352G	5V Industrial (-40°C to 85°C)
20,000-30,000	1	AT40K20LV-1AJC AT40K20LV-1BQC AT40K20LV-1DQC AT40K20LV-1EQC AT40K20LV-1FQC AT40K20LV-1BGC	84J 144Q 208Q 240Q 304Q 352G	3V Commercial (0°C to 70°C)
20,000-30,000	1	AT40K20LV-1AJI AT40K20LV-1BQI AT40K20LV-1DQI AT40K20LV-1EQI AT40K20LV-1FQI AT40K20LV-1BGI	84J 144Q 208Q 240Q 304Q 352G	3V Industrial (-40°C to 85°C)

Ordering Information

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
30,000-40,000	1	AT40K30-1AJC AT40K30-1BQC AT40K30-1DQC AT40K30-1EQC AT40K30-1FQC AT40K30-1BGC AT40K30-1CGC	84J 144Q 208Q 240Q 304Q 352G 432G	5V Commercial (0°C to 70°C)
30,000-40,000	1	AT40K30-1AJI AT40K30-1BQI AT40K30-1DQI AT40K30-1EQI AT40K30-1FQI AT40K30-1BGI AT40K30-1CGI	84J 144Q 208Q 240Q 304Q 352G 432G	5V Industrial (-40°C to 85°C)
30,000-40,000	1	AT40K30LV-1AJC AT40K30LV-1BQC AT40K30LV-1DQC AT40K30LV-1EQC AT40K30LV-1FQC AT40K30LV-1BGC AT40K30LV-1CGC	84J 144Q 208Q 240Q 304Q 352G 432G	3.3V Commercial (0°C to 70°C)
30,000-40,000	1	AT40K30LV-1AJI AT40K30LV-1BQI AT40K30LV-1DQI AT40K30LV-1EQI AT40K30LV-1FQI AT40K30LV-1BGI AT40K30LV-1CGI	84J 144Q 208Q 240Q 304Q 352G 432G	3.3V Industrial (-40°C to 85°C)

Ordering Information

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
40,000-50,000	1	AT40K40-1AJC AT40K40-1BQC AT40K40-1DQC AT40K40-1EQC AT40K40-1FQC AT40K40-1BGC AT40K40-1CGC AT40K40-1AUC	84J 144Q 208Q 240Q 304Q 352G 432G 475U	5V Commercial (0°C to 70°C)
40,000-50,000	1	AT40K40-1AJI AT40K40-1BQI AT40K40-1DQI AT40K40-1EQI AT40K40-1FQI AT40K40-1BGI AT40K40-1CGI AT40K40-1AUI	84J 144Q 208Q 240Q 304Q 352G 432G 475U	5V Industrial (-40°C to 85°C)
40,000-50,000	1	AT40K40LV-1AJC AT40K40LV-1BQC AT40K40LV-1DQC AT40K40LV-1EQC AT40K40LV-1FQC AT40K40LV-1BGC AT40K40LV-1CGC AT40K40LV-1AUC	84J 144Q 208Q 240Q 304Q 352G 432G 475U	3.3V Commercial (0°C to 70°C)
40,000-50,000	1	AT40K40LV-1AJI AT40K40LV-1BQI AT40K40LV-1DQI AT40K40LV-1EQI AT40K40LV-1FQI AT40K40LV-1BGI AT40K40LV-1CGI AT40K40LV-1AUI	84J 144Q 208Q 240Q 304Q 352G 432G 475U	3.3V Industrial (-40°C to 85°C)

Ordering Information

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
5,000-10,000	2	AT40K05-2AJC AT40K05-2AQC AT40K05-2BQC AT40K05-2DQC	84J 100Q 144Q 208Q	5V Commercial (0°C to 70°C)
5,000-10,000	2	AT40K05-2AJI AT40K05-2AQI AT40K05-2BQI AT40K05-2DQI	84J 100Q 144Q 208Q	5V Industrial (-40°C to 85°C)
5,000-10,000	2	AT40K05LV-2AJC AT40K05LV-2AQC AT40K05LV-2BQC AT40K05LV-2DQC	84J 100Q 144Q 208Q	3.3V Commercial (0°C to 70°C)
5,000-10,000	2	AT40K05LV-2AJI AT40K05LV-2AQI AT40K05LV-2BQI AT40K05LV-2DQI	84J 100Q 144Q 208Q	3.3V Industrial (0°C to 70°C)

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
10,000-20,000	2	AT40K10-2AJC AT40K10-2AQC AT40K10-2BQC AT40K10-2DQC AT40K10-2EQC	84J 100Q 144Q 208Q 240Q	5V Commercial (0°C to 70°C)
10,000-20,000	2	AT40K10-2AJI AT40K10-2AQI AT40K10-2BQI AT40K10-2DQI AT40K10-2EQI	84J 100Q 144Q 208Q 240Q	5V Industrial (-40°C to 85°C)
10,000-20,000	2	AT40K10LV-2AJC AT40K10LV-2AQC AT40K10LV-2BQC AT40K10LV-2DQC AT40K10LV-2EQC	84J 100Q 144Q 208Q 240Q	3.3V Commercial (0°C to 70°C)
10,000-20,000	2	AT40K10LV-2AJI AT40K10LV-2AQI AT40K10LV-2BQI AT40K10LV-2DQI AT40K10LV-2EQI	84J 100Q 144Q 208Q 240Q	3.3V Industrial (-40°C to 85°C)

Ordering Information

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
20,000-30,000	2	AT40K20-2AJC AT40K20-2BQC AT40K20-2DQC AT40K20-2EQC AT40K20-2FQC AT40K20-2BGC	84J 144Q 208Q 240Q 304Q 352G	5V Commercial (0°C to 70°C)
20,000-30,000	2	AT40K20-2AJI AT40K20-2BQI AT40K20-2DQI AT40K20-2EQI AT40K20-2FQI AT40K20-2BGI	84J 144Q 208Q 240Q 304Q 352G	5V Industrial (-40°C to 85°C)
20,000-30,000	2	AT40K20LV-2AJC AT40K20LV-2BQC AT40K20LV-2DQC AT40K20LV-2EQC AT40K20LV-2FQC AT40K20LV-2BGC	84J 144Q 208Q 240Q 304Q 352G	3V Commercial (0°C to 70°C)
20,000-30,000	2	AT40K20LV-2AJI AT40K20LV-2BQI AT40K20LV-2DQI AT40K20LV-2EQI AT40K20LV-2FQI AT40K20LV-2BGI	84J 144Q 208Q 240Q 304Q 352G	3V Industrial (-40°C to 85°C)

Ordering Information

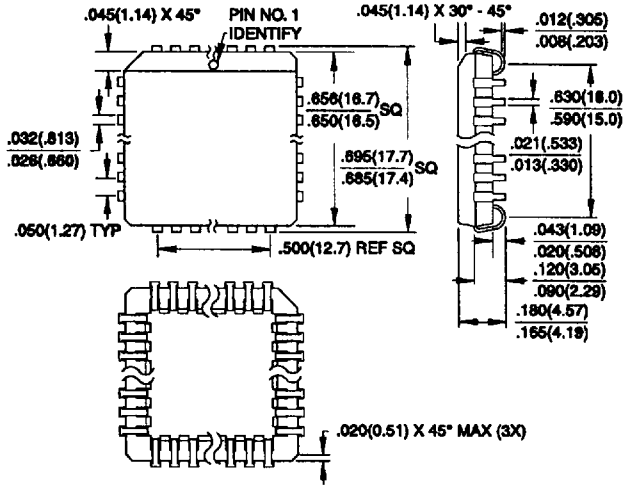
Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
30,000-40,000	2	AT40K30-2AJC AT40K30-2BQC AT40K30-2DQC AT40K30-2EQC AT40K30-2FQC AT40K30-2BGC AT40K30-2CGC	84J 144Q 208Q 240Q 304Q 352G 432G	5V Commercial (0°C to 70°C)
30,000-40,000	2	AT40K30-2AJI AT40K30-2BQI AT40K30-2DQI AT40K30-2EQI AT40K30-2FQI AT40K30-2BGI AT40K30-2CGI	84J 144Q 208Q 240Q 304Q 352G 432G	5V Industrial (-40°C to 85°C)
30,000-40,000	2	AT40K30LV-2AJC AT40K30LV-2BQC AT40K30LV-2DQC AT40K30LV-2EQC AT40K30LV-2FQC AT40K30LV-2BGC AT40K30LV-2CGC	84J 144Q 208Q 240Q 304Q 352G 432G	3.3V Commercial (0°C to 70°C)
30,000-40,000	2	AT40K30LV-2AJI AT40K30LV-2BQI AT40K30LV-2DQI AT40K30LV-2EQI AT40K30LV-2FQI AT40K30LV-2BGI AT40K30LV-2CGI	84J 144Q 208Q 240Q 304Q 352G 432G	3.3V Industrial (-40°C to 85°C)

Ordering Information

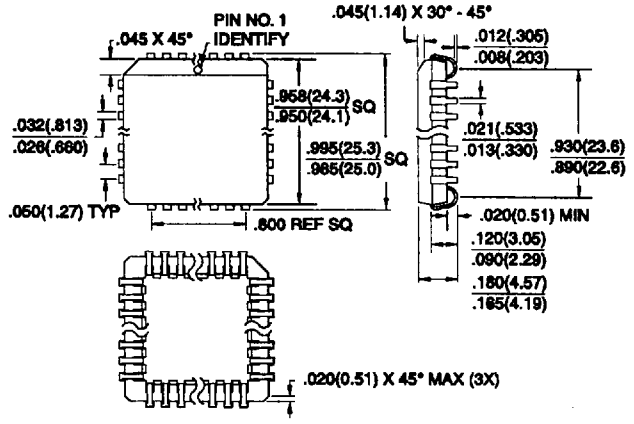
Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
40,000-50,000	2	AT40K40-2AJC AT40K40-2BQC AT40K40-2DQC AT40K40-2EQC AT40K40-2FQC AT40K40-2BGC AT40K40-2CGC AT40K40-2AUC	84J 144Q 208Q 240Q 304Q 352G 432G 475U	5V Commercial (0°C to 70°C)
40,000-50,000	2	AT40K40-2AJI AT40K40-2BQI AT40K40-2DQI AT40K40-2EQI AT40K40-2FQI AT40K40-2BGI AT40K40-2CGI AT40K40-2AUI	84J 144Q 208Q 240Q 304Q 352G 432G 475U	5V Industrial (-40°C to 85°C)
40,000-50,000	2	AT40K40LV-2AJC AT40K40LV-2BQC AT40K40LV-2DQC AT40K40LV-2EQC AT40K40LV-2FQC AT40K40LV-2BGC AT40K40LV-2CGC AT40K40LV-2AUC	84J 144Q 208Q 240Q 304Q 352G 432G 475U	3.3V Commercial (0°C to 70°C)
40,000-50,000	2	AT40K40LV-2AJI AT40K40LV-2BQI AT40K40LV-2DQI AT40K40LV-2EQI AT40K40LV-2FQI AT40K40LV-2BGI AT40K40LV-2CGI AT40K40LV-2AUI	84J 144Q 208Q 240Q 304Q 352G 432G 475U	3.3V Industrial (-40°C to 85°C)

Package Type	
84J	84-Lead, Plastic J-Leaded Chip Carrier (PLCC)
100Q	100-Lead, Very Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (AQFP)
144Q	144-Lead, Thin (1.4 mm) Plastic Gull Wing Quad Flate Package (PQFP)
160Q	160-Lead, Plastic Gull Wing Quad Flate Package (PQFP)
208Q	208-Lead, Plastic Gull Wing Quad Flate Package (PQFP)
225G	225-Lead, Ball Grid Array Package (BGA)
240Q	240-Lead, Plastic Gull Wing Quad Flate Package (PQFP)
304Q	304-Lead, Plastic Gull Wing Quad Flate Package (PQFP)
352G	352-Lead, Ball Grid Array Package (BGA)
432G	432-Lead, Ball Grid Array Package (BGA)
475U	475-Lead, Ceramic Pin Grid Array Package (PGA)

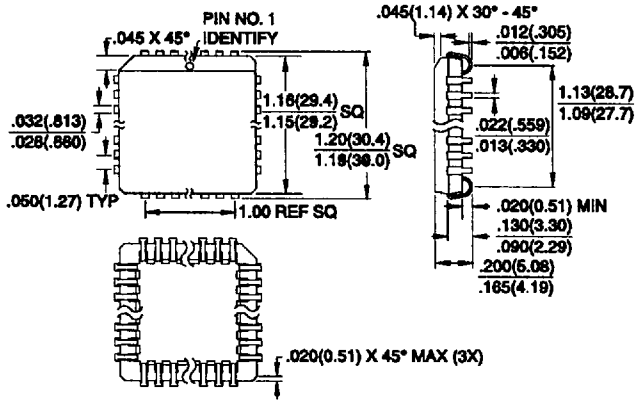
44J, 44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AC



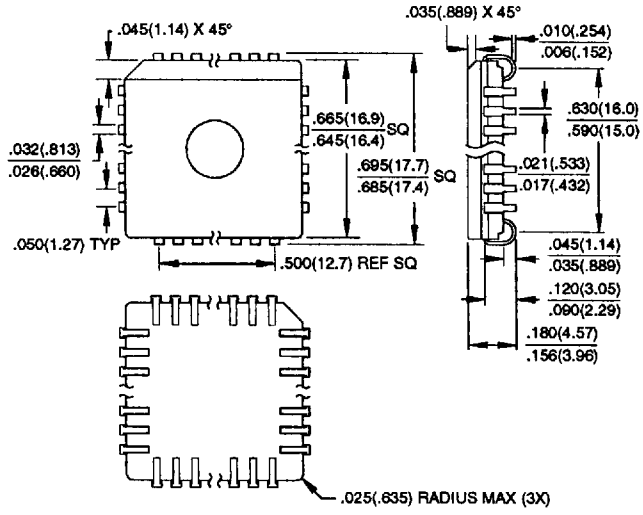
68J, 68 Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AE



84J, 84 Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AF

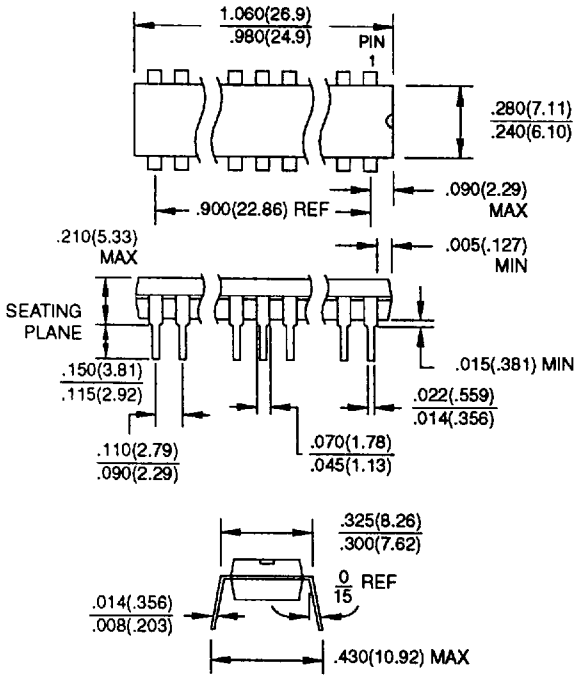


44KW, 44 Lead, Windowed,
Ceramic Leadless Chip Carrier (JLCC)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 C-J1

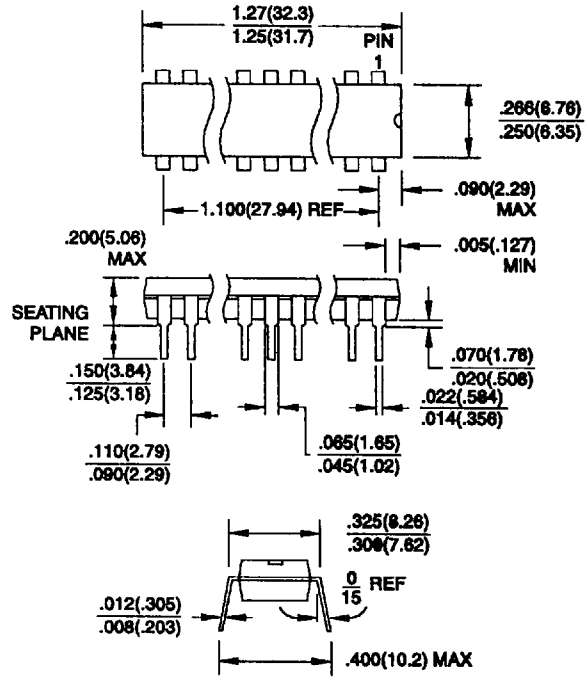


*Ceramic lid standard unless specified.

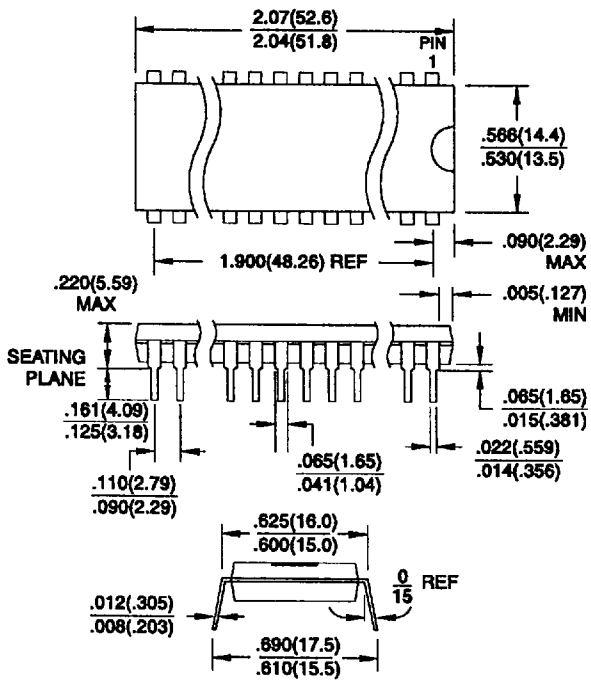
20P3, 20 Lead, 0.300" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-001 AD



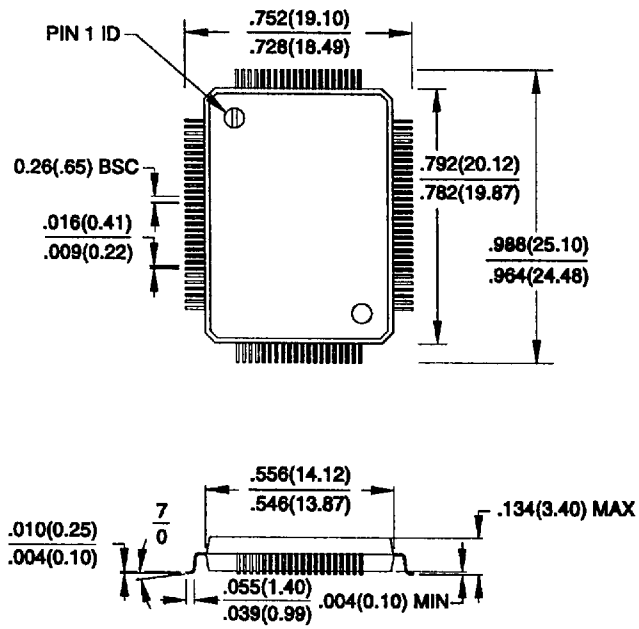
24P3, 24 Lead, 0.300" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-001 AF



40P6, 40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AC

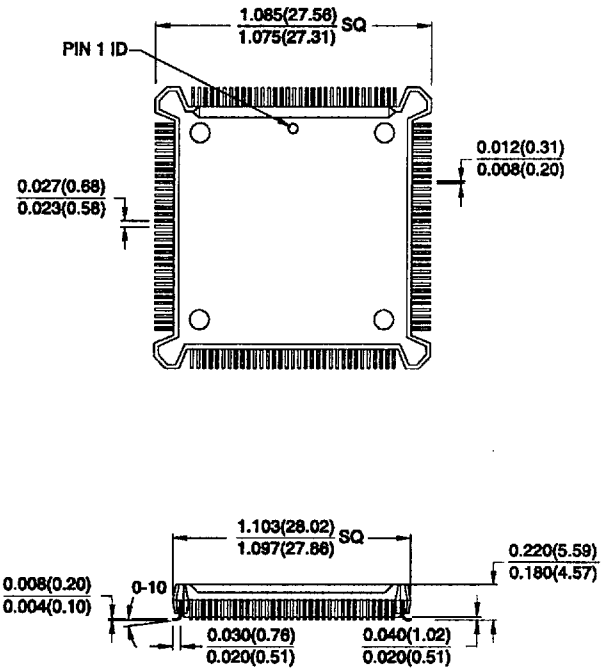


100Q, 100 Lead, Plastic Gull Wing Quad Flat Package (PQFP)
Dimensions in (Millimeters) and Inches



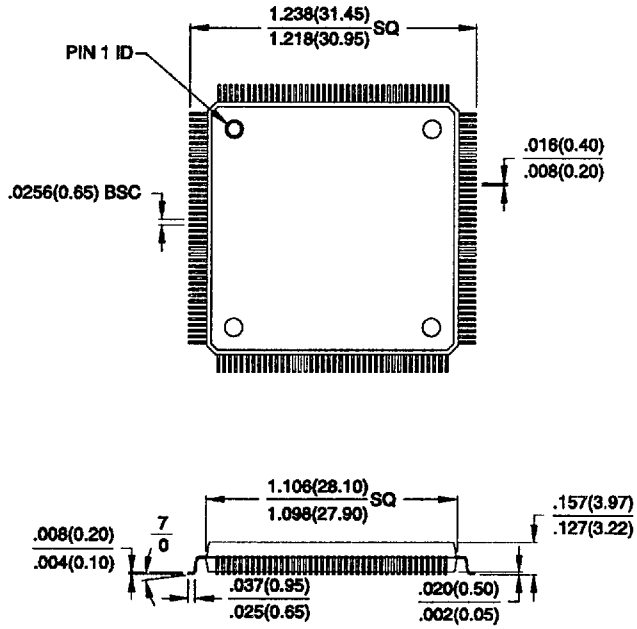
*Controlling dimension: millimeters

132Q, 132 Lead, Bumpered Plastic Gull Wing Quad Flat Package (BQFP)
Dimensions in (Millimeters) and Inches



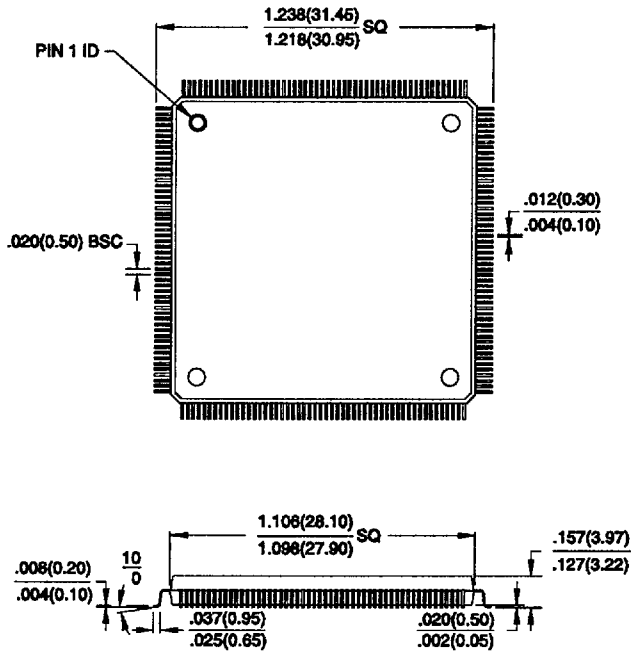
*Controlling dimension: millimeters † FPGA Pin 1

160Q, 160 Lead, Plastic Gull Wing Quad Flat Package (PQFP)
Dimensions in (Millimeters) and Inches



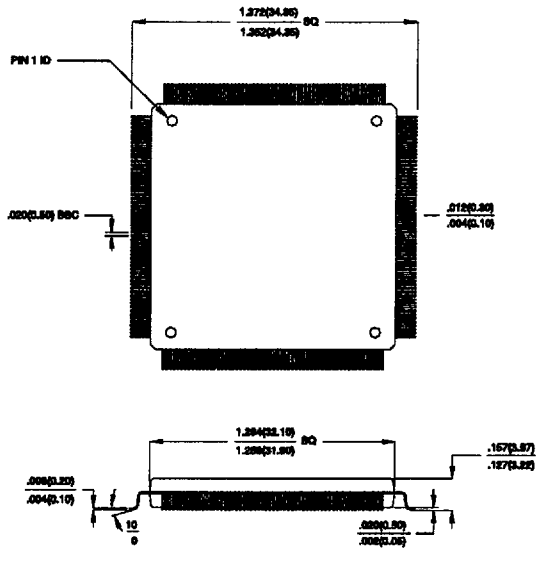
*Controlling dimension: millimeters

208Q, 208 Lead, Plastic Gull Wing Quad Flat Package (PQFP)
Dimensions in (Millimeters) and Inches



*Controlling dimension: millimeters

240Q, 240 Lead, Plastic Gull Wing Quad Flat Package (PQFP)
Dimensions in (Millimeters) and Inches



*Controlling dimension: millimeters